PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2003-004697

(43)Date of publication of application : 08.01.2003

(51)Int.Cl. G01N 27/414
H01L 29/786

(21)Application number : 2001-389680

(22)Date of filing : 21.12.2001

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(30)Priority

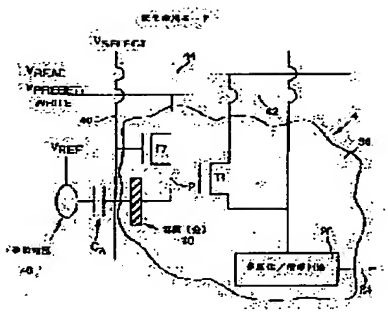
Priority number : 2000 200031716 Priority date : 22.12.2000 Priority country : GB

(54) SENSOR CELL

(57)Abstract:

PROBLEM TO BE SOLVED: To identify a sample that is received by a sensor cell by utilizing the operation of transistors.

SOLUTION: The sensor cell comprises receiving means, which may be in the form of an electrode 10 coupled to a thin-film transistor T1. A voltage supplied to the gate electrode of the transistor T via a switching transistor T7 is controlled according to a capacitance value CA being generated by an electrode according to the reception of a target sample for identification.



LEGAL STATUS

[Date of request for examination] 25.06.2004

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

CLAIMS

[Claim(s)]
[Claim 1] The sensor cel which has a thin film transistor and the acceptance means combined with the gate electrode of said thin film transistor for receiving the sample for identification.
[Claim 2] The sensor cel characterized by being constituted according to the value of the electrostatic capacity which said acceptance means possesses the electrode for samples, and produces in said electrode for samples in a sensor cel according to claim 1 according to acceptance by said electrode for samples of said sample for identification so that actuation of said thin film transistor may be controlled.
[Claim 3] The sensor cel characterized by to constitute said electrode for samples and said criteria capacitor as an electrostatic-capacity dividing network combined with the gate electrode of said thin film transistor for controlling the amplitude of the electrical-potential-difference pulse outputted to said gate electrode according to the value of said electrostatic capacity produced in said electrode for samples in the sensor cel which is a sensor cel according to claim 2, and has a criteria capacitor.
[Claim 4] The sensor cel characterized by being under the metal layer in which said criteria capacitor contacts said gate electrode and said gate electrode, and extends in a sensor cel according to claim 3, and having the pad field separated from said metal layer by the insulator layer.
[Claim 5] The sensor cel characterized by said pad field containing a metal or the doped polish recon in a sensor cel according to claim 4.
[Claim 6] The sensor cel characterized by providing the further transistor for outputting said electrical-potential-difference pulse to the gate electrode of said thin film transistor according to the pulse for selection outputted to the further transistor in a sensor cel given in claim 3 thru/or any 1 term of 5.
[Claim 7] The sensor cel characterized by said further transistor containing a thin film transistor in a sensor cel according to claim 6.
[Claim 8] The sensor cel characterized by being constituted so that it may change according to the value of the electrostatic capacity which the magnitude of the electrical potential difference supplied to the gate electrode of said thin film transistor produces in said electrode for samples by the switching transistor of said switch-on, when the switching transistor for changing between switch-on and non-switch-on is provided in a sensor cel according to claim 2 and said switching transistor is changed to said non-switch-on.
[Claim 9] a sensor cel according to claim 8 -- setting -- said conductor -- the sensor cel characterized by providing the line for selection for outputting the pulse for selection for changing said switching transistor between a condition and said non-switch-on to the gate electrode of said switching transistor.
[Claim 10] The line for presetting for supplying an electrical potential difference to the gate electrode of said thin film transistor in a sensor cel according to claim 9, The object for read-out for the lines for supplying a read-out electrical potential difference to said thin film transistor is provided. A presetting cycle is made possible by outputting said pulse for selection to said switching transistor. Said switching transistor is changed to switch-on by it, and supply of said electrical potential difference to the gate electrode of said thin film transistor is enabled. Subsequently By making a read-out cycle possible and changing said switching transistor to said non-switch-on by it by ending said pulse for selection The magnitude of the electrical potential difference in the gate electrode of said thin film transistor changes,

and it is characterized by said thin film transistor being changed to non-switch-on by this change. Termination of said pulse for selection, The sensor cel characterized by being constituted so that it may therefore decide on the time amount required between the changes to said non-switch-on of said thin film transistor as the value of the electrostatic capacity in said electrode for samples.

[Claim 11] The sensor cel characterized by providing the switching means which combines selectively a threshold voltage compensating circuit including the constant current source which supplies the current of presetting level through said thin film transistor, and said thin film transistor and said constant current source in a sensor cel given in claim 3 thru/or any 1 term of 7.

[Claim 12] In a sensor cel according to claim 11, the transistor of the addition combined with said thin film transistor is provided. When said electrical-potential-difference pulse is outputted to the gate electrode of said thin film transistor and said constant current source is subsequently disconnected from said thin film transistor, The sensor cel characterized by the magnitude of the output current from said thin film transistor consisting of the 1st level determined according to said constant current source so that it may change to the 2nd level therefore determined as the value of the electrostatic capacity produced in said electrode for samples.

[Claim 13] The sensor cel characterized by providing a means to opt for change between said 1st level and said 2nd level of the output current from said thin film transistor, in a sensor cel according to claim 12.

[Claim 14] The sensor cel characterized by said switching means possessing a thin film transistor switching circuit in a sensor cel given in claim 11 thru/or any 1 term of 13.

[Claim 15] The sensor cel characterized by said acceptance means containing gold, silver, or platinum in any 1 term of the above-mentioned claim in the sensor cel of a publication.

[Claim 16] The sensor cel characterized by being constituted so that said acceptance means may receive said sample in the location which said acceptance means is formed in the location which does not overlap said thin film transistor in a sensor cel given in any 1 term of the above-mentioned claim, and does not cover the gate field of said thin film transistor.

[Claim 17] In a sensor cel according to claim 1 or 2, the well part in which said thin film transistor is prepared in said acceptance means into a wrap passivation layer is provided. By it It is characterized by constituting the layer which contacts said gate electrode and consists the extending metal layer of a wrap passivation ingredient. With the charge which said layer which consists of a passivation ingredient has a certain thickness, consequently produces in said well part by acceptance by said well part of said sample for identification The sensor cel characterized by accomplishing so that the electrical potential difference which shows said sample may be produced in the gate electrode of said thin film transistor.

[Claim 18] The sensor cel characterized by including a plastic plate or a glass substrate in any 1 term of the above-mentioned claim in the sensor cel of a publication.

[Claim 19] The sensor characterized by providing the array which changes from the row and column of the sensor cel of a publication to any 1 term of the above-mentioned claim.

[Claim 20] The sensor characterized by providing the line selection register which chooses the line of the sensor cel of said array, and the train selection register which chooses the train of the sensor cel of said array in a sensor according to claim 19.

[Claim 21] The sensor characterized by providing a magnification means to amplify the output signal from said sensor cel, in a sensor according to claim 19 or 20.

[Claim 22] The sensor characterized by providing a multiplexing means to multiplex the output signal from said sensor cel in a sensor given in claim 19 thru/or any 1 term of 21.

[Claim 23] The sensor characterized by providing a comparison means to compare with the output signal and said reference value from a sensor cel a storing means to store the reference value which shows a reference sample, and the display means constituted so that it may be shown whether the sample for identification is in agreement with a reference sample in a sensor given in claim 19 thru/or any 1 term of 22.

[Claim 24] In the sensor of a publication, each sensor cel possesses a reference electrode in claim 19 thru/or any 1 term of 23. It is constituted so that two or more reference electrodes arranged by the relation estranged through said array may support the common reference matter. The sensor which receives an output signal and is characterized by having further a circuit means to equalize from the sensor cel containing one in said two or more reference electrodes which support said common reference matter.

[Claim 25] The approach characterized by having the step which establishes the sensor cel containing a thin film transistor, and the acceptance means combined with the gate electrode of said thin film transistor which receives said sample in the approach of identifying a sample.

[Claim 26] The approach characterized by having the step which forms said acceptance means in the location which does not overlap said thin film transistor in order that said acceptance means may receive said sample in an approach according to claim 25 in the location which does not cover the gate field of said thin film transistor.

[Claim 27] The approach which is an approach according to claim 25 or 26, and is characterized by controlling actuation of said thin film transistor according to the value of the electrostatic capacity produced in said electrode for samples according to acceptance by the electrode for samples of said sample in the approach of having the step which establishes said acceptance means as an electrode for samples.

[Claim 28] The approach characterized by having the step which controls the amplitude of the electrical-potential-difference pulse outputted to said gate electrode according to the value of said electrostatic capacity which forms a criteria capacitor, constitutes said criteria capacitor and said electrode for samples in an approach according to claim 27 as an electrostatic-capacity dividing network combined with the gate electrode of said thin film transistor, and is produced in said electrode for samples.

[Claim 29] The approach which contacts said gate electrode and is characterized by being under the extending metal layer and having the step which forms said criteria capacitor as a pad field separated from said metal layer by the insulator layer in an approach according to claim 28.

[Claim 30] The approach characterized by having the step which prepares said pad field as a field which consists of the polish recon which consisted of the metal or was doped in the approach according to claim 29.

[Claim 31] The approach characterized by having the step which prepares the further transistor, and the step which controls said electrical-potential-difference pulse outputted to said gate electrode by impressing the pulse for selection to said further transistor in an approach according to claim 28.

[Claim 32] The approach characterized by having the step which prepares said further transistor as a thin film transistor in an approach according to claim 31.

[Claim 33] The step which combines the switching transistor and said electrode for samples for performing the change between switch-on and non-switch-on in an approach according to claim 27, Said electrode for samples is combined with the step which said switching transistor operates by said switch-on, and supplies an electrical potential difference to the gate electrode of said thin film transistor with said switching transistor. By it The approach characterized by having the step which changes according to the value of the electrostatic capacity which the magnitude of the electrical potential difference supplied to the gate electrode of said thin film transistor produces in said electrode for samples when said switching transistor is changed to said non-switch-on.

[Claim 34] The approach characterized by changing said switching transistor between said un-flowing and said switch-on in an approach according to claim 33 by outputting the pulse for selection to said switching transistor from the line for selection.

[Claim 35] The line for presetting for supplying an electrical potential difference to the gate electrode of said thin film transistor in an approach according to claim 34, It has the step which prepares the line for read-out for supplying a read-out electrical potential difference to said thin film transistor. By this A

presetting cycle is made possible by outputting said pulse for selection to said switching transistor. Said switching transistor is changed to switch-on by said presetting cycle, and said electrical potential difference is supplied to the gate electrode of said thin film transistor. Subsequently By terminating said pulse for selection, a read-out cycle is made possible and said switching transistor is changed to said non-switch-on by this read-out cycle. By this change The magnitude of the electrical potential difference in the gate electrode of said thin film transistor changes, and it is characterized by being made as [change / by this change / to non-switch-on / said thin film transistor]. Termination of said pulse for selection, The approach characterized by therefore deciding on the time amount required between the changes of said thin film transistor to said non-switch-on as the value of the electrostatic capacity in said electrode for samples.

[Claim 36] The approach characterized by having the step which prepares a threshold voltage compensating circuit including the constant current source which supplies the current of the level which flows the inside of said thin film transistor, and by which presetting was carried out, and the switching means which combines said constant current source with said thin film transistor selectively in an approach given in claim 28 thru/or any 1 term of 30.

[Claim 37] The step which combines an additional transistor with said thin film transistor in an approach according to claim 36, Said constant current source is disconnected from the step which outputs said electrical-potential-difference pulse to the gate electrode of said thin film transistor, and said thin film transistor. By this cutting The approach characterized by having the step which changes the magnitude of the output current from said thin film transistor from the 1st level determined according to said constant current source to the 2nd level therefore determined as the value of the electrostatic capacity produced in said electrode for samples.

[Claim 38] In an approach according to claim 25 or 26, contact said gate electrode, and the extending metal layer so that the layer which consists of a wrap passivation ingredient may be prepared It is characterized by having the step which establishes said acceptance means as a well part constituted in a wrap passivation layer in said thin film transistor. With the charge which said layer which consists of a passivation ingredient has a certain thickness, consequently produces in said well part by acceptance by said well part of said sample for identification The approach characterized by accomplishing so that the electrical potential difference which shows said sample may be produced in the gate electrode of said thin film transistor.

[Claim 39] The approach characterized by having the step which manufactures said sensor cel on the substrate which changes from plastics or glass to claim 25 thru/or any 1 term of 37 in the approach of a publication.

[Claim 40] The approach characterized by having the step which prepares two or more sensor cels constituted as an array which changes from the row and column of a sensor cel to claim 25 thru/or any 1 term of 38 in the approach of a publication.

[Claim 41] The approach characterized by having the step which prepares the line selection register which chooses said line of a sensor cel in said array in an approach according to claim 40, and prepares the train selection register which chooses the train of a sensor cel in said array.

[Claim 42] The approach characterized by having the step which establishes a magnification means to amplify the output signal from said sensor cel, in an approach according to claim 40 or 41.

[Claim 43] The approach characterized by having the step which establishes a multiplexing means to multiplex the output signal from said sensor cel in an approach given in claim 40 thru/or any 1 term of 42.

[Claim 44] The chemical sensor characterized by providing the sensor of a publication in a sensor cel given in claim 1 thru/or any 1 term of 18 or claim 19 thru/or any 1 term of 24.

[Claim 45] Fingerprint recognition equipment characterized by providing the sensor of a publication in a sensor cel given in claim 1 thru/or any 1 term of 18 or claim 19 thru/or any 1 term of 24.

[Claim 46] Operating instructions of the biosensor which has the approach of a publication in claim 25

thru/or any 1 term of 43.
[Claim 47] Operating instructions of the fingerprint recognition equipment characterized by having the approach of a publication in claim 25 thru/or any 1 term of 43.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001] This invention relates to the sensor which unified a sensor cel and such a sensor cel.
[0002] The chemical sensor with which the array which consists of the sensor cel containing a semi-conductor transistor was unified is known. Generally by such sensor, the silicon wafer has been used as a substrate ingredient. However, silicon is an expensive ingredient relatively, and since a biosensor can use it only once by disposal in the case of a type of a certain kind of sensor still like a biosensor, it poses a problem with the especially important abolition nature of the sensor after an activity. When silicon is used as a substrate ingredient, the disposal of a used biosensor poses a still more troublesome problem.
[0003] In addition, it is known that the difficulty relevant to manufacture of the transistor array on a silicon substrate will increase remarkably with buildup of array size. For this reason, there is an inclination for the device of the high density which uses a silicon substrate also in the case of the array of which predetermined size to be used. In the case of a biosensor, just this high recording density may pose a problem. It is because there are requirements that the active part of the micro electro nick chip which unified the array must operate in a wet environment in much application.
[0004] The chemical sensor of many forms, such as a biosensor, is proposed. In the multi-biosensor of one type, pH sensor of the array form which consists of four ion-sensitive field-effect transistors (ISFET) combined with four metal oxide film field-effect transistors (MOSFET) which function as a source follower circuit possesses. However, in order to perform insulation sufficient between ISFET(s), in the proposed array, size becomes what was relatively bulky. furthermore, ISFET is one form of a transistor, and in case it insulates such a device from a solvent to be examined, ****** in ** produce it. In order that some may solve the problem of this insulation, the method of manufacturing ISFET and MOSFET on a silicon layer in the form of the separate field of the shoes supported on silicon on sapphire is proposed. Sapphire was used as a substrate ingredient for the outstanding electrical insulating characteristic. Subsequently, a protective coat is formed in an ISFET gate front face, and the film which induces a compound to be examined, respectively continues after that. Thus, it is also possible to use it in order for each formed sensor to function as a pH sensor and to perform detection of a urea, a glucose, and a potassium. However, as mentioned above, this sensor array had comparatively large size, and when it was 4 sensor array, it was width of face of 2mm, and size with a die length of 6mm mostly. Furthermore, while silicon on sapphire is applicable to manufacture of an array

only to a certain fixed size and array size becomes large, it is well-known data that the problem relevant to the array manufacture by silicon activity increases substantially. Furthermore, since the silicon substrate ingredient and especially the substrate ingredient that consists of sapphire are relatively expensive, the chemical sensor of the above-mentioned type becomes what has a very high manufacturing cost. When it takes into consideration that the sensor of many types can use it only once by disposal, the side face of this cost is an especially troublesome problem. Furthermore, since these ingredients cannot be discarded easily, a serious problem will be produced on an environment about the disposal after an activity.

[0005] Recently, utilization of a submicron CMOS technology was proposed as a biosensor array for DNA analysis. With this technique, manufacture of the array which consists of about 1000 sensor cels on the substrate of the size of number square millimeter order was attained. However, since a CMOS device is manufactured on a silicon substrate, the proposed array will have high recording density. In order to insulate an active CMOS device from wet operating environment, the integrated mold reaction checking chamber (integratedreaction test chamber) of dedication of the cavity form arranged between two printed circuits by which sealing closure was piled up, set and carried out is prepared. The DNA ingredient for analysis is separated into the 2 chain by heating, and, subsequently an indicator is attached with a fluorescence molecule using biochemical processing. Subsequently, the specimen containing a DNA strand contacts a chip and is arranged. When one DNA strand has the array which is in agreement with a target's (target) array established on the electrode of a sensor, hybridization (hybridization) arises and the physical localization (localization) of the DNA sample to the suitable electrode top of a chip arises as a result. Subsequently, the rinse of the chip is carried out and a sensor is read with a CCD camera. Since the indicator is attached with the fluorescence molecule, as for a DNA strand, the generating part of association (bonding) is shown by the relative brightness on the electrode of a device. The compatibility of the ingredient for conveying a sentiment chip concept (wet-chip concept) with high dependability, manufacture, and a package are recognized as an important trouble about the applicability of such a device. These troubles can aim at eclectic solution by the requirements that high recording density must be attained on a silicon substrate ingredient. Moreover, such a biosensor becomes what has a high manufacturing cost relatively so that clearly from the above-mentioned explanation.

[0006] Since comparatively cheap non-silicon substrates, such as soda glass and plastics, can be used for a thin film transistor (TFT), a manufacturing cost becomes cheap relatively. Since it is the ingredient in which disposal is possible relatively, utilization of a plastic plate can give an additional advantage. Furthermore, TFT can be easily manufactured as an array of a large area, and such a technique is in industry in manufacture of for example, an active-matrix mold liquid crystal display etc., and is already used widely. Therefore, the production process is fully proved and can obtain relatively the device [in low cost] which can operate the high yield with high dependability especially as compared with a silicon substrate device. Consideration of that the array of an area larger than an available array can be manufactured with high dependability from a silicon substrate increases these advantages further. It is thought that there is a very big problem in using a silicon wafer substrate as an object for the arrays of such a large area. It is mentioned that originate in the substrate ingredient itself and semi-conductor manufacturing technology which must be adopted inevitably as the reason, and manufacture of an array becomes increasingly difficult, and cost becomes high.

[0007] In order to detect a certain kind of matter, in case such a device is used, a fault also exists in relation to the engine performance of the device. Generally the comparison-film which consists of the silicon dioxide (SiO2) supported on the doped silicon substrate is contained in MOSFET. This SiO two-layer has the proper electrostatic capacity inversely proportional to the thickness of a layer. When preparing SiO two-layer by the typical thickness of about 100nm, remarkable loss of an electrostatic-capacity nature signal arises from a device. This loss originates in SiO two-layer proper electrostatic capacity. When preparing SiO two-layer as a film dramatically and aiming at an improvement of a signal

output, a device becomes instability dramatically during an activity. If the electrode for detection is made very small, it will become mitigable [conflict in these designs]. However, since the electrode for detection is what is used in order to receive the quality of an identification object, it needs to manufacture the electrode for detection in usable size actually. Therefore, although it is necessary to take the comparatively large gate field of MOSFET, by prepare a comparatively large gate field, the recording density of the transistor which can be hold on the silicon substrate of finite size will decrease substantially, and the problem on the fundamental manufacture in connection with utilization of the silicon transistor as an object for chemical sensors will arise in that this reduction will reduce the number of the sensor cels which can be shortly hold in a sensor array.

[0008] As for the dominant factor at the time of a device design, since the need of attaining very high recording density does not become especially in the case of a chemical sensor or a biosensor, it shows a remarkable advantage at a comparatively cheap price for manufacture of TFT to be easily possible as an array of a large area as compared with the silicon device currently used conventionally. Therefore, the field relevant to each sensor cel of the array which receives the sample for identification becomes possible [moving from a location with the component of an active semi-conductor], when required, and the problem of the insulation which exists about the present silicon substrate device is solved for some. Furthermore, the detection field (the form of the electrode for DNA sensors may be carried out) which receives the sample for identification becomes possible [making it the thing of comparatively large size], a detection field is expanded, and an improvement of the engine performance is achieved. Furthermore, it becomes possible to reduce the pack density of TFT from the pack density seen with much present application which is using these devices, and another advantage will be given by utilization of this expanded detection field in that lifting of the yield of the device which functions thoroughly can be acquired from the existing production process.

[0009] It is known that TFT shows mobility lower than a silicon substrate transistor, and when manufacturing TFT as a transistor device which consists of the array of a large area which is the special advantage of a biosensor, TFT may show fluctuation of the transfer characteristics between the transistors in an array. These fluctuation becomes remarkable, and in order to identify one sample especially, when it is a DNA biosensor with many samples necessary [to be analyzed] general vitally, the array of a large area serves as an advantage which meaning has in reduction of time amount required for sample analysis dramatically, as array size becomes large.

[0010] So, when use the electrostatic capacity produce between an electrode and the sample for identification as the measurement technique, the potential fault relevant to the variability of the engine performance of TFT be solve, and I be further understand as a gestalt with suitable for this invention make such a device usable easily as an active device for chemical sensors of the form of the array of a large area which consist of a sensor cel.

[0011] By using TFT as an object for chemical sensors, the production capacity of the array of a large area which the advantage on the cost which surpasses the activity of a silicon substrate device is not only acquired, but has the improved detection field will also be obtained. Furthermore, the significant additional advantage of the improved abolition nature is also produced. This advantage is an advantage especially important for a biosensor device or a chemical sensor device in the reason such a device may be used only once by disposal as mentioned above.

[0012] Therefore, it is the object of this invention to offer the improved sensor cel which uses a thin film transistor. Furthermore, it is the objects of this invention to use detection of the electrostatic capacity in the electrode produced from the electrode which receives the sample for identification as the measurement technique, and to use this electrostatic capacity further, in order to control actuation of a thin film transistor.

[0013] According to the 1st mode of this invention, the sensor cel possessing the acceptance means of the sample for identification combined with the gate electrode of a thin film transistor and a thin film transistor is offered.

[0014] With a suitable configuration, the above-mentioned sensor cel possesses a criteria capacitor, the electrode for samples and a criteria capacitor are constituted as an electrostatic-capacity dividing network (capacitance divider circuit) combined with the gate electrode of a thin film transistor, and this dividing network is prepared as an object for control of the amplitude of the electrical-potential-difference pulse outputted to a gate electrode according to the value of the electrostatic capacity produced with the electrode for samples.
[0015] With structure with a suitable sensor cel, a criteria capacitor possesses the pad field under a gate electrode and the gate electrode separated from this gate electrode by the insulator layer.
[0016] It is desirable to be constituted so that actuation of a thin film transistor may be controlled according to the electrostatic-capacity value which the above-mentioned acceptance means possesses the electrode for samples, and produces in the electrode for samples suitably according to acceptance by the electrode for samples of the sample for identification.
[0017] It is constituted so that it may become small according to the value of the electrostatic capacity which the magnitude of the electrical potential difference outputted to a gate electrode by the switching transistor by switch-on when the switching transistor to which a sensor cel changes between non-[switch-on and] switch-on with a substitute configuration is provided, a gate electrode is further contained in a thin film transistor and a switching transistor is changed to non-switch-on produces in the electrode for samples.
[0018] The line for selection where a sensor cel outputs the pulse for selection for changing a switching transistor between switch-on and non-switch-on in this 1st mode of this invention suitably, The line for writing which supplies an electrical potential difference to the gate electrode of a thin film transistor, It has the line for read-out which supplies a read-out (read) electrical potential difference to a thin film transistor. A write cycle becomes possible by outputting the pulse for selection to a switching transistor. A switching transistor is changed to switch-on by this write cycle. Supply of the electrical potential difference to the control gate of a thin film transistor is enabled. In that case By a read-out cycle's becoming possible and performing the change to the non-switch-on of a switching transistor by this read-out cycle by terminating the pulse for selection It is desirable to be constituted so that the magnitude of the electrical potential difference in the gate electrode of a thin film transistor may change, a thin film transistor may be changed to non-switch-on by this change and supply of the output signal from a thin film transistor may be terminated. Therefore, it decides on the time amount required between termination of the pulse for selection, and the change of the thin film transistor to non-switch-on as the value of the electrostatic capacity in the electrode for samples.
[0019] Suitably, as for a sensor cel, it is desirable that a threshold voltage compensating circuit (threshold voltage compensation) including the constant current source which supplies the current of the presetting level which flows the inside of a film transistor, and the switching means which combines this constant current source with a thin film transistor selectively can be included.
[0020] When the transistor of the addition by which the sensor cel was combined with the thin film transistor is provided most suitably, an electrical-potential-difference pulse is outputted to the gate electrode of a thin film transistor and a constant current source is disconnected from a thin film transistor, it is desirable for the magnitude of the output current from a thin film transistor to consist of the 1st level determined according to the constant current source so that it may change to the 2nd level according to the value of the electrostatic capacity produced in the electrode for samples.
[0021] It is desirable to become the configuration that an acceptance means receives a sample in the location which the above-mentioned acceptance means is suitably constituted by the location which does not overlap a thin film transistor, and does not cover the gate field of a thin film transistor.
[0022] Suitably, it is desirable to manufacture a sensor cel on a plastic plate. According to the 2nd mode of this invention, the sensor possessing the array which consists of the row and column of a sensor cel according to the 1st mode of this invention is offered.
[0023] According to the 3rd mode of this invention, the identification approach of the sample which has

the step which prepares the sensor cel containing a thin film transistor and the electrode for samples which receives a sample, and the step which controls actuation of a thin film transistor according to the value of the electrostatic capacity produced from sample acceptance by the electrode for samples in the electrode for samples is offered.

[0024] Suitably, as for the above-mentioned identification approach, it is desirable to have the step which controls the amplitude of the electrical-potential-difference pulse outputted to a gate electrode according to the value of the step which forms a criteria capacitor, the step which constitutes this criteria capacitor and the electrode for samples as an electrostatic-capacity dividing network combined with the gate electrode of a thin film transistor, and the electrostatic capacity produced in the electrode for samples.

[0025] In the 2nd mode of the above of this invention, suitably the above-mentioned approach The step which combines the switching transistor which performs the change between switch-on and non-switch-on, and the electrode for samples, The electrode for samples is combined with the step which makes a switching transistor switch-on and supplies an electrical potential difference to the gate electrode of a thin film transistor with a switching transistor. By it When a switching transistor is changed to non-switch-on, it is desirable to have the step which changes according to the value of the electrostatic capacity which the magnitude of the electrical potential difference supplied to the gate electrode of a thin film transistor produces in the electrode for samples.

[0026] A switching transistor is suitably changed between non-switch-on by outputting the pulse for selection to a switching transistor from the line for selection. The line for writing for supplying an electrical potential difference to the gate electrode of a thin film transistor, The line for read-out for supplying a read-out electrical potential difference to a thin film transistor is prepared. By outputting the pulse for selection to a switching transistor, a write cycle is made possible and a switching transistor is changed to switch-on by this write cycle. By this change Output an electrical potential difference to the control gate of a thin film transistor, and a read-out cycle is further made possible by terminating the pulse for selection. A switching transistor is changed to non-switch-on by this read-out cycle. By this change The magnitude of the electrical potential difference in the gate electrode of a thin film transistor is changed, a thin film transistor is changed to non-switch-on by the change, and the output signal from a thin film transistor is terminated. Termination of the pulse for selection, It is desirable to decide on the time amount required between the changes of the thin film transistor to non-switch-on as the value of the electrostatic capacity in the electrode for samples therefore.

[0027] It is desirable to have most suitably the step at which the above-mentioned approach prepares a thin film transistor on a plastic plate.

[0028] It is desirable for the above-mentioned approach to combine an additional transistor with a thin film transistor suitably, to output an electrical-potential-difference pulse to the gate electrode of a thin film transistor, to disconnect a constant current source from a thin film transistor, and for this to also have the step which changes the magnitude of the output current acquired from a thin film transistor to the 2nd level determined according to the value of the electrostatic capacity produced from the 1st predetermined level determined according to the constant current source in the electrode for samples.

[0029] According to the 4th mode of this invention, the sensor according to the 2nd mode of the biosensor possessing the sensor cel according to the 1st mode of this invention or this invention is offered.

[0030] According to the 5th mode of this invention, the fingerprint recognition equipment possessing the sensor according to the 2nd mode of the sensor cel according to the 1st mode of this invention or this invention is offered.

[0031] According to the 6th mode of this invention, the operating instructions of the biosensor according to the 3rd mode of this invention or fingerprint recognition equipment are offered.

[0032] When drawing 1 is referred to, the sensors 2, such as a chemical sensor, are Lines 6 and 6a... They are 6n and Trains 8 and 8a... They are the sensor cels 4a and 4b arranged by 8n... The array which

consists of 4n is provided. A thin film transistor (TFT) T1, an electrode 10, and the further transistor T6 and the further criteria capacitor Cr are contained in each sensor cel 4a. Moreover, the actuation explained below to be the train presetting register 12, the line selection register 14, and the train selection register 16 is also included in a sensor 2. Multiplexing / amplifying circuit 20 which operates under control of another train selection register 22 are formed in order to perform magnification and multiplexing of the output signal from a sensor cel, and an output signal is outputted from a sensor array with the output line 24. Although the electrode 10 is shown by drawing 1 as a plate electrode which receives a fingertip, the electrode in a solution can be similarly included by the electrode 10. The circuit constituted as sensor cel 4a of a graphic display is included in drawing 1 at each of the sensor cel of an array.

[0033] The sensor of the graphic display to drawing 1 operates in steady state detection mode, and the electrical potential difference of the gate electrode 26 of a transistor T1 is determined by the value of the electrostatic capacity produced with the electrode 10 (the capacitor nqtation Cs shows to drawing 1) produced from the electrode 10 which receives the sample for identification combined with the value of the criteria capacitor Cr as a result.

[0034] At the time of initiation of a cycle, the sensor cel within trains, such as a train 8, is beforehand set up by impressing the electrical potential difference from the train presetting register 12 to the line 28 for presetting. The transistor T6 of each cel is turned on, and bias voltage **** is impressed to the gate electrode 26 of a transistor T1. This bias voltage **** is outputted and is [from non-switch-on / change] ready [for switch-on] so that a transistor T1 may be set to the predetermined operating point of that characteristic curve. Moreover, when a consecutiveness pulse is impressed to the gate electrode 26 so that it may explain below, not going up to level with the electrical potential difference of the gate electrode 26 is guaranteed by the above-mentioned change. Such level is the current level which cannot let a transistor T1 pass and which is too high, and is the current of level which will probably destroy a transistor T1.

[0035] The pulse for line selection is outputted to Node N through the criteria capacitor Cr by the activity of the line selection register 14 with a line 30. The pulse for train selection is supplied with a line 32 by the activity of the train selection register 16. Since the pulse for line selection and the pulse for train selection are not outputted at the event of arbitration only to one line and one train, selection of single cels, such as sensor cel 4a of drawing 1 , is attained. For example, it is assumed that sensor 4a receives a fingertip with the fingerprint made into the object of identification. An electrode 10 receives a part of fingertip, and electrode 10a of sensor cel 4b which adjoins [near / in train 8a / immediately] receives the adjacent part of the fingertip. Since the front face of a fingertip functions as a collaboration electrode with Electrodes 10 and 10a, read-out of the value (shown in drawing 1 as Cs) of the electrostatic capacity between a fingertip and each of Electrodes 10 and 10a becomes possible. In order that electrostatic capacity Cs and Cr may make AC divider substantially, when sensor cel 4a receives the pulse for line selection with a line 30, according to the value of the criteria electrostatic capacity Cr, and the value Cs of the electrostatic capacity produced from the fingertip which touched the electrode 10, the magnitude of the electrical potential difference in Node N is changed.

[0036] As mentioned above, bias is almost applied to a transistor T1 to a flowing point by the impression of an electrical potential difference **** to the gate electrode 26. Therefore, when sensor cel 4a is chosen by the impression of the pulse for line selection to a line 30, and the impression of the pulse for train selection to a line 32, the magnitude of the electrical potential difference of the initial value **** in Node P rises to the value determined by the relative values Cs and Cr of electrostatic capacity. Since Cr is a fixed value capacitor, the value of this electrical potential difference is proportional to the value Cs of electrostatic capacity. The value of the output current acquired from a transistor T1 as this natural result will be proportional to the value Cs of electrostatic capacity. Therefore, a thin film transistor T1 will be controlled according to the value of the electrostatic capacity produced with the electrode 10 for samples produced as a result of acceptance by the electrode for samples of the sample

for identification (a part of fingerprint of a fingertip).
[0037] The current of the output line 34 is sent out to multiplexing / amplifying circuit 20. In multiplexing / amplifying circuit 20, the selection signal from the 2nd train selection register 22 is given to the train selection signal and coincidence of a line 32 to a transistor T1. Bias voltage Vbias is outputted to the gate electrode of a transistor T5. Thus, suitable selection of a transistor T1 enables it to perform magnification and multiplexing to up to the output section 24 of the output current of a line 34. Similarly, it is also possible to multiplex the output current from other sensor cels to up to the output section 24.
[0038] When the sensor 2 possesses fingerprint recognition equipment, in the fingertip which contacted the sensor and was placed, Yamabe of a fingerprint pattern in contact with a certain fixed electrode for samples arises, and the trough of a fingerprint pattern in contact with another electrode for samples arises in it. When it assumes that Yamabe of a fingerprint has been received with the electrode 10 and the trough of a fingerprint has been received by electrode 10a, the value Cs of the electrostatic capacity of sensor cel 4a differs from the value Cs of the electrostatic capacity of sensor cel 4b. A thing with the same said of other sensor cels in the array which receives Yamabe of a fingerprint pattern or a trough is applied. Typically, a sensor 4 can possess the sensor cel array of 200x300. Therefore, by taking the suitable timing of the signal from the line selection register 14 and the train selection registers 16 and 22, the sensor cel of an array is scanned continuously and it becomes possible to send out to storage the output signal with which the sensor cel which appears in the output section 24 was multiplexed. By the comparator, it becomes possible to compare with a reference value the value in which these samples were stored, and identification of a fingerprint is attained as a result of such a comparison. The output signal of the output section 24 can also be sent out to the display for displaying a fingerprint image which is detected by the sensor 2.
[0039] It is desirable suitably to manufacture multiplexing / amplifying circuit 20 in one with a sensor 2, and the transistor (transistors T1–T5 are illustrated as the part) of a circuit may possess TFT on a sensor 2 and the common substrate 36 in that case. Each transistor T6 for sensor cels may possess TFT. Although it possesses the suitable charge of supporting material of arbitration, when a substrate 36 manufactures suitably all the transistors that consist of a sensor 2 as TFT, it is desirable for a substrate 36 to contain plastic material.
[0040] Although the steady state detection sensor of a graphic display was explained to drawing 1 in relation to fingerprint recognition equipment, it is also possible to use this steady state detection sensor as a biosensor which performs detection and recognition of DNA, an antibody, etc. of a liquefied biomaterial. In this case, some electrodes which receive the matter in a solution are prepared. It becomes possible to identify special material as compared with a predetermined reference value about the value of the electrostatic capacity produced from this matter.
[0041] Drawing 2 shows the alternative example of the sensor cel according to this invention. The sensor cel of the graphic display to drawing 2 operates in 'change detection (transient detection)' mode, and identification of a sample is performed using the time constant determined with the value of the electrostatic capacity produced from the electrode which receives the DNA sample which is in this 'change detection' mode, for example, is made into the object of identification.
[0042] In the sensor cel 4 of the graphic display to drawing 2 , a switching transistor T7 is combined with an electrode 10, and the node P prepared between the transistor T7 and the electrode 10 is combined with the gate electrode T1 of a thin film transistor. Since a selection signal Vselect, the presetting signal Vpreset, and the read-out signal Vread are outputted, the line 40 for selection, the line 42 for writing, and the line 44 for read-out are formed, respectively. Since an output signal is outputted in the output section 24, multiplexing / amplifying circuit 20 is formed.
[0043] Actuation of the circuit of a graphic display is explained to drawing 2 R> 2 in relation to identification of a liquefied DNA sample. However, by the same approach as the approach explained with reference to drawing 1 , if available, he should understand the change detector of the graphic display to drawing 2 also about the case of fingerprint recognition. In fingerprint detection, the reference electrode

46 of drawing 2 will be constituted by the front face of a fingertip, and the electrical potential difference Vref of drawing 2 will be outputted with the charge generated on the surface of a fingertip.
[0044] The transistors T1 and T7 to which both sides can possess TFT at the time of initiation of an operating cycle are to un-flow, i.e., an OFF condition. An electrode 30 is constituted as an electrode within a suitable container, and is put into liquefied DNA into this container. Since DNA is fixable, it is received with an electrode 10, consequently the electrostatic-capacity value CA produces it between the electrode 10 for samples, and a reference electrode 46.
[0045] The cycle set up beforehand is started and a switching transistor T7 is changed from non-switch-on to switch-on by impressing an electrical potential difference Vselect to the gate electrode of a transistor T7. The electrical potential difference Vpreset set up beforehand is simultaneously supplied to the source electrode of a transistor T7, and the read-out electrical potential difference Vread is impressed to the source electrode of a transistor T1. It goes up to the electrical-potential-difference Vpreset level to which the electrical potential difference in Node P was beforehand set when the transistor T7 was changed to ON, and if the electrical potential difference in Node P exceeds the threshold voltage of a transistor T1, a transistor T1 will change to ON and the current of the output section of a transistor T1 will serve as a function of the electrical potential difference in Node P (gate electrode of a transistor T1).
[0046] Subsequently, by terminating the selection electrical potential difference Vselect, a read-out cycle is started and a transistor T7 is changed to un-flowing [of origin], i.e., an OFF condition. If a transistor T7 is changed to OFF, the electrical potential difference of Node P will fall by leakage through a transistor T7, therefore, it will be determined as the electrostatic-capacity value CA, the rate, i.e., the time constant, which this leakage produces, and, therefore, this electrostatic-capacity value will be further determined as the amount of identifications of the DNA sample which the electrode 10 for samples receives. Interrelative reduction of a current arises in the output section of a thin film transistor T1, and this current is sent out to multiplexing / amplifying circuit 20 as the magnitude of the electrical potential difference in Node P becomes small. When the electrical potential difference in Node P falls below to the threshold voltage of a transistor T1, a transistor T1 changes to OFF and reduces further the current sent out to multiplexing / amplifying circuit 20 to the level of the leakage current which flows the inside of a transistor T1. A transistor T7 is used as a digital switching transistor, and, on the other hand, it is understood from the above-mentioned explanation that a transistor T1 functions as a converter from analog voltage to a current. Therefore, it becomes possible to determine the amount of identifications of the sample which an electrode 10 receives by acting as the monitor of the current therefore determined as the electrostatic-capacity value CA in the output section of a transistor T1.
[0047] In order to use it as a biosensor, the pair of a sensor cel like a graphic display can be prepared in drawing 2 . One cel of a couple functions as a cel for samples, and a pair of another side functions as a reference cel which a reaction did not produce.
[0048] When using the sensor cel of a graphic display for drawing 1 and drawing 2 as a chemical sensor or biosensors (DNA sensor etc.), subsequently it is necessary to write in first the chemistry ingredient and biomaterial which are made into the object of identification into a cel, and to write in up to a reference electrode. This writing can be considered to be the write-in phase of a cel, and is performed suitably at the time of manufacture of a device. the electromagnetism which it is possible to use an ink jet head with sufficient convenience, and to perform adhesion of a chemistry ingredient and a biomaterial, and impresses a charge to an electrode -- by adhesion, adhesion of a up to [an electrode] is assisted and the quality of an affix can be drawn to the adhesion part of a request of an electrode.
[0049] Drawing 3 is drawing showing the embodiment of available semi-conductor structure, in order to form a thin film transistor T1, an electrode 10, and the criteria capacitor Cr.
[0050] The layer which consists of the polish recon 48 is contained in the TFT structure of drawing 3 , and this polish recon layer is suitably supported by the substrate 36 with desirable it being the ingredient which consists of plastics or a soda glass ingredient. The gate electrode 26 is formed on the

polish recon layer 48, and is separated from a polish recon layer by the insulating layer 50 which consists of a silicon dioxide. The gate electrode 26 is covered with the passivation layers (passivation layer) 52 and 54.

[0051] An insulating layer 50 and the gate electrode 26 are a wrap about the pad field 56 which consists of the metal or the doped polish recon which was constituted so that it might extend in the field whole polish recon layer 48, and was formed on the substrate 36. The well extended below is established in the passivation layers 52 and 54, and exposure of the gate electrode 26 is performed in a wrap field in the pad field 56. The electrode 10 which may be a thing containing gold, silver, or platinum extends below, and is formed into the well in contact with the gate electrode 26. Thus, a criteria capacitor is formed between the pad field 56 and the gate electrode 26. By drawing 3 , the criteria capacitor is shown by the dotted line as an example.

[0052] Moreover, without being contradictory to the need of attaining the maximum recording density on an expensive silicon substrate ingredient, since it is not what unified TFT and unified the silicon substrate transistor, the structure of the graphic display to drawing 3 can arrange an electrode 10 so that TFT may not be overlapped. An electrode 10 is constituted so that the gate field of TFT may not be covered as a result. Therefore, an electrode 10 becomes possible [considering as the electrode of the amplification size which can aim at an improvement of device sensibility], and becomes possible [manufacturing more easily enclosure required in order to insulate TFT from the wet environment further produced in an electrode with higher dependability]. It is because the requirements that the high recording density of a device must be attained on an expensive substrate do not exist.

[0053] Drawing 3 shows that the compact configuration which unified the thin film transistor T1, the electrode 10, and the criteria capacitor Cr is given according to this structure. Consequently, it becomes possible to unify this structure in the steady state detection sensor cel of drawing 1 . If the sample for identification is received with an electrode 10, the value Cs of the electrostatic capacity of the graphic display to drawing 3 produced between an electrode 10 and a sample will be combined with the indispensable criteria capacitor Cr, and the electrostatic-capacity dividing network explained with reference to drawing 1 will be formed. Actuation of TFT is controlled by this dividing network.

[0054] To drawing 2 , in the case of the change detection sensor cel of a graphic display, since the criteria capacitor is unnecessary, the pad field 56 can be excluded.

[0055] As mentioned above, there is fluctuation of threshold voltage as one trouble about poly-Si TFT. This fluctuation is compensated and the alternative circuit of the sensor cel which supplies the output which is equal to an output from TFT over the substrate of a large area is illustrated by drawing 4 R> 4.

[0056] In the sensor cel of drawing 4 , a thin film transistor T1 is combined with either a constant current source Isource or an output line through Switch S. The additional transistor T8 which operates as a switching transistor is connected between the gate of a thin film transistor T1, and a drain electrode, and the criteria capacitor Cr is connected between the gate of a transistor T1, and a source electrode. The electrode (not shown to drawing 4) which receives the sample for identification is also combined with the gate electrode of a transistor T1. Therefore, the electrostatic-capacity divider equipped with the criteria capacitor Cr with the sample electrostatic capacity Cs is formed by the approach explained with reference to drawing 1 , and the same approach.

[0057] If a transistor T8 is turned on, the electrical potential difference VGS from the gate to the source of a transistor T1 and the electrical potential difference VDS from a drain to the source will become equal. Under such conditions, the operating characteristic of a transistor T1 is simplified, as shown in drawing 5 . When Switch S is in a location "1", the current from a constant current source Isource is lengthened through a transistor T1, and the result of the voltage drop VDSref covering the ends of a transistor T1 arises. Since the transistor T8 is turned on (therefore, VGS is equal to VDS in the case of a transistor T1), the voltage drop VDSref produced over the ends of a transistor T1 is stored into the criteria capacitor Cr.

[0058] The threshold shift in a thin film transistor T1 may produce the result of the shift of the

operating characteristic curve by which the transistor T1 was simplified like the graphic display to drawing 6 (when VGS is equal to VDS). Since the value of the current which flows the inside of a transistor T1 is supplied from a constant current source and Isource, it is fixed. Therefore, the result of change of the voltage drop VDSref which is produced between the power source of a transistor T1 and a drain electrode in any case of the threshold shift will be produced. An electrical potential difference VDSref is stored into the criteria capacitor Cr. Therefore, the electrical potential difference VGS between the gate electrode of a transistor T1 and a source electrode is beforehand charged by this value. Thus, presetting of the transistor T1 is carried out to the predetermined operating point of the characteristic curve.

[0059] Next, although it becomes equal to a current from a constant current source Isource at first since the current Iout of an output line is governed by the electrical potential difference in Node P when Switch S is moved to a location "2" and T8 is changed to OFF, subsequently to the criteria capacitor Cr, the stored electrical potential difference rules over. Subsequently, when a voltage source Vref performs a pulse output, the electrical potential difference in Node P rises, and a pulse is outputted according to an electrical potential difference Vref. The current Iout of an output line outputs a pulse according to lifting of the electrical potential difference of Node P.

[0060] Since a capacity divider is formed of the criteria capacitor Cr and electrostatic capacity Cs, lifting of the electrical potential difference in the node P in case a voltage source Vref outputs a pulse is determined by the relative electrostatic-capacity value of Cr and Cs. Lifting of the output current Iout from the initial value of the output current equal to a current from a constant current source Isource can be measured, and the value Cs of the electrostatic capacity which shows the sample which the electrode for samples has received can be quantified.

[0061] He can understand that Switch S may be formed by the switching means by semiconductor device like the thin film transistor on a substrate 36.

[0062] Drawing 7 illustrates another example of this invention which can use this sensor as a pH sensor. Since the structure of the graphic display to drawing 7 is dramatically similar to drawing 3 with the structure of a graphic display, it is made into the thing of this structure for which a part is shown similarly using the same possible reference number.

[0063] With the structure of the graphic display to drawing 7 , a well 58 is established in the passivation layer 52, and exposure of the gate electrode 26 is performed. The passivation layer 54 is formed into a well 58 as the passivation layer 52 and a continuation layer which extends over the gate electrode 26 top, it crosses on a gate electrode, and the comparison-film which consists of the passivation ingredient 60 is prepared. It is put into the object sample to which identification is performed in the form of solutions, such as a urea and a glucose, into a well 58, a layer 60 is contacted, the ion in a solution approaches a layer 60, and the proton shown with + notation by drawing 7 is absorbed by the front face 62 of a layer 60. Since a layer 60 is dramatically thin, the electrical potential difference which controls actuation of the TFT transistor which this charge moves to the gate electrode 60, consequently is constituted by the gate electrode 26, the polish recon field 48, and the silicon dioxide layer 50 is outputted. The charge made by adsorption of the ion to a front-face 62 top in the layer 60 relates to pH of the solution which adhered into the well 58. Therefore, it becomes possible by acting as the monitor of the output from TFT to identify the matter in a solution.

[0064] This contractor is just going to understand that it is possible to correct without giving the above-mentioned explanation as a mere example, and deviating from the range of this invention.

[0065] As an example, the sensor cel was explained in relation to detection of a liquefied chemistry ingredient or a biomaterial. However, if it is also possible to analyze fluids other than liquids, such as a gas, using a sensor cel, he should understand.

[0066] Furthermore, this invention was explained in relation to one sensor cel used for analysis of a specific chemistry ingredient or a biomaterial sample. However, TFT is high dependability as compared with a silicon substrate device, and since it can manufacture to the array of a very large area, it can

prepare some sensor cels to which each has the specific DNA train written in up to the reference electrode in the matrix of the sensor cel which constitutes a sensor. The output signal acquired from these sensor cels that have common reference matter written in up to a reference electrode, such as a DNA train, when such a cel is prepared by the relation estranged and arranged over the ends of an array is equalized by suitable circuitry, and becomes possible [inducing a high analysis precision]. This analysis circuitry may be manufactured on a substrate using TFT. Thus, it becomes possible to prepare in a sensor some 'duplicate' sensor cels intrinsically constituted so that each may identify a common DNA character string. The above thing becomes possible using TFT, because it is possible to unify many sensor cels in the array of a very large area dramatically.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The sensor according to the 1st example of this invention is illustrated.
[Drawing 2] The sensor according to the 2nd example of this invention is illustrated.
[Drawing 3] The structure of the sensor cel used for drawing 1 by the sensor of a graphic display is illustrated.
[Drawing 4] A sensor cel including fluctuation of the threshold voltage used for drawing 1 by the sensor of a graphic display is illustrated.
[Drawing 5] The operating characteristic by which the thin film transistor of the sensor cel of a graphic display was simplified by drawing 4 is illustrated.
[Drawing 6] The fluctuation of the operating characteristic by which the graphic display was simplified by drawing 5 to which the threshold voltage of a thin film transistor is changed is illustrated.
[Drawing 7] The alternative structure of the sensor cel used as a pH sensor according to this invention is illustrated.

[Translation done.]

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報**（Ａ）　(11)特許出願公開番号
特開2003－4697
（P2003－4697A）
(43)公開日　平成15年１月８日(2003.1.8)

(51)Int.Cl.'	識別記号	ＦＩ	テーマコード'（参考）
Ｇ０１Ｎ　27/414		Ｇ０１Ｎ　27/30	３０１Ｙ　５Ｆ１１０
Ｈ０１Ｌ　29/786			３０１Ｘ
		Ｈ０１Ｌ　29/78	６２５
			６１３Ｚ

審査請求　未請求　請求項の数47　ＯＬ　外国語出願　（全 50 頁）

(21)出願番号　特願2001－389680(P2001－389680)
(22)出願日　平成13年12月21日(2001.12.21)
(31)優先権主張番号　００３１７１６．４
(32)優先日　平成12年12月22日(2000.12.22)
(33)優先権主張国　イギリス（ＧＢ）

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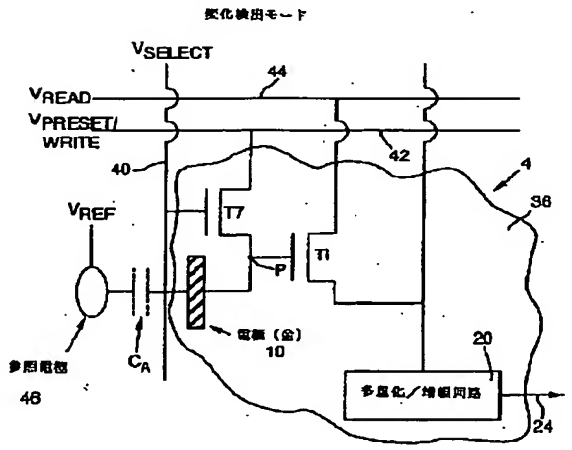
最終頁に続く

(54)【発明の名称】　センサ・セル

(57)【要約】　（修正有）
【課題】トランジスタの動作を利用して、センサ・セルにより受容されたサンプルの同定を提供する。
【解決手段】センサ・セルが受容手段を具備し、該受容手段は、薄膜トランジスタＴ１と結合された電極１０の形状を成すものであって、スイッチング・トランジスタＴ７を介してトランジスタＴ１のゲート電極へ供給される電圧は、同定対象サンプルの受容により電極で生じる静電容量値C_Aに従って制御される。



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【特許請求の範囲】

【請求項１】　薄膜トランジスタと、同定対象サンプルを受容するための、前記薄膜トランジスタのゲート電極と結合された受容手段とを有するセンサ・セル。

【請求項２】　請求項１に記載のセンサ・セルにおいて、前記受容手段がサンプル用電極を具備し、前記同定対象サンプルの前記サンプル用電極による受容に応じて前記サンプル用電極において生じる静電容量の値に従って、前記薄膜トランジスタの動作を制御するように構成されることを特徴とするセンサ・セル。

【請求項３】　請求項２に記載のセンサ・セルであって、基準コンデンサを有するセンサ・セルにおいて、前記サンプル用電極において生じる前記静電容量の値に従って、前記ゲート電極に対して出力される電圧パルスの振幅を制御するための、前記薄膜トランジスタのゲート電極と結合された静電容量分割回路として前記サンプル用電極と前記基準コンデンサとが構成されることを特徴とするセンサ・セル。

【請求項４】　請求項３に記載のセンサ・セルにおいて、前記基準コンデンサが、前記ゲート電極と、前記ゲート電極と接触して延在する金属層の下にあって、絶縁体層によって前記金属層から分離された埋込み領域とを有することを特徴とするセンサ・セル。

【請求項５】　請求項４に記載のセンサ・セルにおいて、前記埋込み領域が金属またはドープされたポリシリコンを含むことを特徴とするセンサ・セル。

【請求項６】　請求項３乃至５のいずれか１項に記載のセンサ・セルにおいて、さらなるトランジスタへ出力される選択用パルスに応じて前記薄膜トランジスタのゲート電極へ前記電圧パルスを出力するためのさらなるトランジスタを具備することを特徴とするセンサ・セル。

【請求項７】　請求項６に記載のセンサ・セルにおいて、前記さらなるトランジスタが薄膜トランジスタを含むことを特徴とするセンサ・セル。

【請求項８】　請求項２に記載のセンサ・セルにおいて、導通状態と非導通状態との間で切替えを行うためのスイッチング・トランジスタを具備し、前記スイッチング・トランジスタが前記非導通状態へ切り替えられたとき、前記導通状態のスイッチング・トランジスタによって前記薄膜トランジスタのゲート電極へ供給される電圧の大きさが、前記サンプル用電極において生じる静電容量の値に従って変化するように構成されることを特徴とするセンサ・セル。

【請求項９】　請求項８に記載のセンサ・セルにおいて、前記導体状態と前記非導通状態との間で前記スイッチング・トランジスタを切り替えるための選択用パルスを前記スイッチング・トランジスタのゲート電極へ出力するための選択用ラインを具備することを特徴とするセンサ・セル。

【請求項１０】　請求項９に記載のセンサ・セルにおいて、前記薄膜トランジスタのゲート電極へ電圧を供給するためのプリセット用ラインと、前記薄膜トランジスタへ読出し電圧を供給するための読出し用ライン用とを具備し、前記スイッチング・トランジスタへ前記選択用パルスを出力することによりプリセット・サイクルを可能にし、それによって前記スイッチング・トランジスタを導通状態へ切り替えて前記薄膜トランジスタのゲート電極への前記電圧の供給を可能にし、次いで、前記選択用パルスを終了することにより読出しサイクルを可能にし、それによって前記スイッチング・トランジスタを前記非導通状態へ切り替えることにより、前記薄膜トランジスタのゲート電極での電圧の大きさが変化し、該変化により非導通状態へ前記薄膜トランジスタが切り替えられることを特徴とし、前記選択用パルスの終了と、前記薄膜トランジスタの前記非導通状態への切替えとの間で要する時間が前記サンプル用電極における静電容量の値に依って決定されるように構成されることを特徴とするセンサ・セル。

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【請求項１１】　請求項３乃至７のいずれか１項に記載のセンサ・セルにおいて、前記薄膜トランジスタを介してプリセット・レベルの電流を供給する定電流源を含む閾値電圧補償回路と、前記薄膜トランジスタと前記定電流源とを選択的に結合するスイッチ手段とを具備することを特徴とするセンサ・セル。

【請求項１２】　請求項１１に記載のセンサ・セルにおいて、前記薄膜トランジスタと結合された追加のトランジスタを具備し、前記薄膜トランジスタのゲート電極へ前記電圧パルスが出力され、次いで前記定電流源が前記薄膜トランジスタから切断されたとき、前記薄膜トランジスタからの出力電流の大きさが、前記定電流源により決定される第１のレベルから、前記サンプル用電極において生じる静電容量の値に依って決定される第２のレベルへ変化するように構成されることを特徴とするセンサ・セル。

【請求項１３】　請求項１２に記載のセンサ・セルにおいて、前記薄膜トランジスタからの出力電流の前記第１のレベルと前記第２のレベルとの間の変化を決定する手段を具備することを特徴とするセンサ・セル。

【請求項１４】　請求項１１乃至１３のいずれか１項に記載のセンサ・セルにおいて、前記スイッチ手段が薄膜トランジスタ・スイッチ回路を具備することを特徴とするセンサ・セル。

【請求項１５】　上記請求項のいずれか１項に記載のセンサ・セルにおいて、前記受容手段が金、銀あるいはプラチナを含むことを特徴とするセンサ・セル。

【請求項１６】　上記請求項のいずれか１項に記載のセンサ・セルにおいて、前記受容手段が前記薄膜トランジスタとオーバーラップしない位置に設けられ、前記薄膜トランジスタのゲート領域を覆わない位置で前記受容手段が前記サンプルを受容するように構成されることを特

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徴とするセンサ・セル。

【請求項１７】　請求項１または２に記載のセンサ・セルにおいて、前記受容手段が前記薄膜トランジスタを覆う不動態化層の中に設けられる井戸部分を具備し、それによって、前記ゲート電極と接触して延在する金属層を覆う不動態化材料から成る層が構成されることを特徴とし、不動態化材料から成る前記層が或る厚さを有し、その結果、前記同定対象サンプルの前記井戸部分による受容により前記井戸部分において生じる電荷によって、前記サンプルを示す電圧が前記薄膜トランジスタのゲート電極において生み出されるように為すことを特徴とするセンサ・セル。

【請求項１８】　上記請求項のいずれか１項に記載のセンサ・セルにおいて、プラスチック基板またはガラス基板を含むことを特徴とするセンサ・セル。

【請求項１９】　上記請求項のいずれか１項に記載のセンサ・セルの行と列とから成るアレイを具備することを特徴とするセンサ。

【請求項２０】　請求項１９に記載のセンサにおいて、前記アレイのセンサ・セルの行を選択する行選択レジスタと、前記アレイのセンサ・セルの列を選択する列選択レジスタとを具備することを特徴とするセンサ。

【請求項２１】　請求項１９または２０に記載のセンサにおいて、前記センサ・セルからの出力信号を増幅する増幅手段を具備することを特徴とするセンサ。

【請求項２２】　請求項１９乃至２１のいずれか１項に記載のセンサにおいて、前記センサ・セルからの出力信号を多重化する多重化手段を具備することを特徴とするセンサ。

【請求項２３】　請求項１９乃至２２のいずれか１項に記載のセンサにおいて、参照サンプルを示す参照値を格納する格納手段と、センサ・セルからの出力信号と前記参照値とを比較する比較手段と、同定対象サンプルが参照サンプルに一致するかどうかを示すように構成される表示手段とを具備することを特徴とするセンサ。

【請求項２４】　請求項１９乃至２３のいずれか１項に記載のセンサにおいて、各センサ・セルが参照電極を具備し、前記アレイを通じて離間した関係で配置される複数の参照電極が共通の対照標準物質を担持するように構成され、前記共通の対照標準物質を担持する前記複数の参照電極の中の１つを含むセンサ・セルから出力信号を受容し、平均化する回路手段をさらに有することを特徴とするセンサ。

【請求項２５】　サンプルを同定する方法において、薄膜トランジスタを含むセンサ・セルと、前記サンプルを受容する前記薄膜トランジスタのゲート電極と結合された受容手段とを設けるステップを有することを特徴とする方法。

【請求項２６】　請求項２５に記載の方法において、前記受容手段が、前記薄膜トランジスタのゲート領域を覆

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わない位置で前記サンプルを受容するために、前記薄膜トランジスタとオーバーラップしない位置に前記受容手段を設けるステップを有することを特徴とする方法。

【請求項２７】　請求項２５または２６に記載の方法であって、サンプル用電極として前記受容手段を設けるステップを有する方法において、前記サンプルのサンプル用電極による受容に応じて前記サンプル用電極において生じる静電容量の値に従って前記薄膜トランジスタの動作が制御されることを特徴とする方法。

【請求項２８】　請求項２７に記載の方法において、基準コンデンサを設け、前記薄膜トランジスタのゲート電極と結合された静電容量分割回路として前記基準コンデンサと前記サンプル用電極とを構成し、前記サンプル用電極において生じる前記静電容量の値に従って、前記ゲート電極へ出力される電圧パルスの振幅を制御するステップを有することを特徴とする方法。

【請求項２９】　請求項２８に記載の方法において、前記ゲート電極と接触して延在する金属層の下にあって、絶縁体層によって前記金属層から分離された埋込み領域として前記基準コンデンサを設けるステップを有することを特徴とする方法。

【請求項３０】　請求項２９に記載の方法において、金属から成るまたはドープされたポリシリコンから成る領域として前記埋込み領域を設けるステップを有することを特徴とする方法。

【請求項３１】　請求項２８に記載の方法において、さらなるトランジスタを設けるステップと、前記さらなるトランジスタに対して選択用パルスを印加することにより、前記ゲート電極へ出力される前記電圧パルスの制御を行うステップとを有することを特徴とする方法。

【請求項３２】　請求項３１に記載の方法において、薄膜トランジスタとして前記さらなるトランジスタを設けるステップを有することを特徴とする方法。

【請求項３３】　請求項２７に記載の方法において、導通状態と非導通状態との間の切替えを行うためのスイッチング・トランジスタと前記サンプル用電極とを結合するステップと、前記導通状態で前記スイッチング・トランジスタが作動して前記薄膜トランジスタのゲート電極へ電圧を供給するステップと、前記サンプル用電極を前記スイッチング・トランジスタと結合し、それによって、前記スイッチング・トランジスタが前記非導通状態へ切り替えられたとき、前記薄膜トランジスタのゲート電極へ供給される電圧の大きさが、前記サンプル用電極において生じる静電容量の値に従って変化するステップと、を有することを特徴とする方法。

【請求項３４】　請求項３３に記載の方法において、選択用ラインから前記スイッチング・トランジスタへ選択用パルスを出力することにより、前記非導通と前記導通状態との間で前記スイッチング・トランジスタを切り替えることを特徴とする方法。

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【請求項３５】　請求項３４に記載の方法において、前記薄膜トランジスタのゲート電極へ電圧を供給するためのプリセット用ラインと、前記薄膜トランジスタへ読出し電圧を供給するための読出し用ラインとを設けるステップとを有し、これによって、前記選択用パルスを前記スイッチング・トランジスタへ出力することによりプリセット・サイクルを可能にし、前記プリセット・サイクルによって前記スイッチング・トランジスタを導通状態へ切り替えて、前記薄膜トランジスタのゲート電極へ前記電圧を供給し、次いで、前記選択用パルスを終了させることにより読出しサイクルを可能にし、該読出しサイクルによって前記スイッチング・トランジスタを前記非導通状態へ切り替え、この切替えにより、前記薄膜トランジスタのゲート電極における電圧の大きさが変化し、該変化によって前記薄膜トランジスタが非導通状態へ切り替えられるようになされることを特徴とし、前記選択用パルスの終了と、前記非導通状態への前記薄膜トランジスタの切替えとの間で要する時間が、前記サンプル用電極における静電容量の値に依って決定されることを特徴とする方法。

【請求項３６】　請求項２８乃至３０のいずれか１項に記載の方法において、前記薄膜トランジスタの中を流れるプリセットされたレベルの電流を供給する定電流源と、前記定電流源を選択的に前記薄膜トランジスタと結合するスイッチ手段とを含む閾値電圧補償回路を設けるステップを有することを特徴とする方法。

【請求項３７】　請求項３６に記載の方法において、追加のトランジスタを前記薄膜トランジスタと結合するステップと、前記薄膜トランジスタのゲート電極へ前記電圧パルスを出力するステップと、前記薄膜トランジスタから前記定電流源を切断し、該切断によって、前記定電流源によって決定された第１のレベルから、前記サンプル用電極において生じる静電容量の値に依って決定される第２のレベルへ前記薄膜トランジスタからの出力電流の大きさを変化させるステップと、を有することを特徴とする方法。

【請求項３８】　請求項２５または２６に記載の方法において、前記ゲート電極と接触して延在する金属層を覆う不動態化材料から成る層が設けられるように、前記薄膜トランジスタを覆う不動態化層の中に構成される井戸部分として前記受容手段を設けるステップを有することを特徴とし、不動態化材料から成る前記層が或る厚さを有し、その結果、前記同定対象サンプルの前記井戸部分による受容により前記井戸部分において生じる電荷によって、前記サンプルを示す電圧が前記薄膜トランジスタのゲート電極において生み出されるように為すことを特徴とする方法。

【請求項３９】　請求項２５乃至３７のいずれか１項に記載の方法において、プラスチックまたはガラスから成る基板上に前記センサ・セルを製造するステップを有することを特徴とする方法。

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【請求項４０】　請求項２５乃至３８のいずれか１項に記載の方法において、センサ・セルの行と列とから成るアレイとして構成される複数のセンサ・セルを設けるステップを有することを特徴とする方法。

【請求項４１】　請求項４０に記載の方法において、センサ・セルの前記行を選択する行選択レジスタを前記アレイに設け、センサ・セルの列を選択する列選択レジスタを前記アレイに設けるステップを有することを特徴とする方法。

【請求項４２】　請求項４０または４１に記載の方法において、前記センサ・セルからの出力信号を増幅する増幅手段を設けるステップを有することを特徴とする方法。

【請求項４３】　請求項４０乃至４２のいずれか１項に記載の方法において、前記センサ・セルからの出力信号を多重化する多重化手段を設けるステップを有することを特徴とする方法。

【請求項４４】　請求項１乃至１８のいずれか１項に記載のセンサ・セル、または、請求項１９乃至２４のいずれか１項に記載のセンサを具備することを特徴とする化学センサ。

【請求項４５】　請求項１乃至１８のいずれか１項に記載のセンサ・セル、または、請求項１９乃至２４のいずれか１項に記載のセンサを具備することを特徴とする指紋認識装置。

【請求項４６】　請求項２５乃至４３のいずれか１項に記載の方法を有するバイオセンサの操作方法。

【請求項４７】　請求項２５乃至４３のいずれか１項に記載の方法を有することを特徴とする指紋認識装置の操作方法。

【発明の詳細な説明】

【０００１】本発明はセンサ・セル、及び、そのようなセンサ・セルを一体化したセンサに関する。

【０００２】半導体トランジスタを含むセンサ・セルから成るアレイが一体化された化学センサが知られている。このようなセンサでは、基板材料として一般にシリコン・ウェーハが使用されてきた。しかし、シリコンは相対的に高価な材料であり、さらに、バイオセンサのような或る種のタイプのセンサの場合、廃棄処分までにバイオセンサが１回しか使用できないため、使用後のセンサの廃棄性が特に重要な問題となる。基板材料としてシリコンが使用される場合、使用済みバイオセンサの廃棄処分はさらに厄介な問題となる。

【０００３】加えて、アレイ・サイズの増大と共に、シリコン基板上でのトランジスタ・アレイの製造に関連する難点が著しく増加することが知られている。このため、いずれの所定サイズのアレイの場合にもシリコン基板を用いる高密度のデバイスが使用される傾向がある。バイオセンサの場合この高い記録密度こそが問題となる

場合がある。というのは、多くのアプリケーションでは、アレイを一体化したマイクロエレクトロニック・チップのアクティブ部分がウェット環境で作動しなければならないという要件があるからである。

【０００４】バイオセンサなどの多くの形の化学センサが提案されている。１つのタイプのマルチバイオセンサでは、ソース・フォロワ回路として機能する４つの金属酸化膜電界効果トランジスタ（ＭＯＳＦＥＴ）と組み合わされた４つのイオン感応電界効果トランジスタ（ＩＳＦＥＴ）から成るアレイ形のｐＨセンサが具備されている。しかし、ＩＳＦＥＴ間で十分な絶縁を行うために、提案されたアレイではサイズが相対的に嵩張ったものとなる。さらに、ＩＳＦＥＴはトランジスタの１つの形であり、このようなデバイスを検査対象溶剤から絶縁する際少なからぬ問題が生じる。この絶縁という問題を多少とも解決するために、サファイア基板上に支持されたいくつかの別々の領域の形でシリコン層上にＩＳＦＥＴとＭＯＳＦＥＴとを製造する方法が提案されている。サファイアが、その優れた電気絶縁特性のために基板材料として使用された。次いでＩＳＦＥＴゲート表面に保護膜が形成され、検査対象化合物にそれぞれ感応する膜がその後に続く。このように形成された個々のセンサはｐＨセンサとして機能し、尿素、グルコース及びカリウムの検出を行うために使用することも可能である。しかし、上述のように、このセンサ・アレイはサイズが比較的大きく、４センサ・アレイの場合ほぼ幅２ｍｍ、長さ６ｍｍのサイズであった。さらに、サファイア基板は、或る一定サイズまでしかアレイの製造には使用できず、アレイ・サイズが大きくなると共に、シリコン使用によるアレイ製造に関連する問題が大幅に増えることは周知の事実である。さらに、シリコン基板材料、及び、特にサファイアから成る基板材料は相対的に高価であるため、上記タイプの化学センサは製造コストが非常に高いものとなる。多くのタイプのセンサが廃棄処分までに１回しか使用できないことを考え合わせると、このコストという側面は特に厄介な問題である。さらに、これらの材料は容易に廃棄できないため、使用後の廃棄処分に関して環境上重大な問題を生じることになる。

【０００５】最近、ＤＮＡ分析用バイオセンサ・アレイとして、サブミクロンＣＭＯＳ技術の利用が提案された。この技術によって、数平方ミリメートルオーダーのサイズの基板上に約１０００個のセンサ・セルから成るアレイの製造が可能となった。しかし、ＣＭＯＳデバイスはシリコン基板上に製造されるため、提案されたアレイは高い記録密度を持つことになる。ウェットな動作環境からアクティブＣＭＯＳデバイスを絶縁するために、２つの重ね合わされ、密閉封止されたプリント配線間に配設されるキャビティ形の専用の統合型反応検査用チャンバ（integratedreaction test chamber）が設けられる。分析対象ＤＮＡ材料は加熱によってその２本鎖に分離され、次いで、生化学的処理を用いて蛍光分子により標識がつけられる。次いで、ＤＮＡ鎖を含む検体がチップと接触して配置される。１本のＤＮＡ鎖が、センサの電極上に設けられた標的（target）の配列に一致する配列を有する場合、ハイブリダイゼーション(hybridization)が生じ、チップの適切な電極上へのＤＮＡサンプルの物理的局在（localization）が結果として生じる。次いで、チップはリンスされ、ＣＣＤカメラでセンサが読み取られる。ＤＮＡ鎖は蛍光分子によって標識がつけられているため、デバイスの電極上の相対的輝度によって結合（bonding）の発生個所が示される。ウェット・チップ・コンセプト（wet-chip concept）を高い信頼性で伝えるための材料の互換性、製造及び包装が、このようなデバイスの適用性に関する重要な問題点として認識されている。これらの問題点は、シリコン基板材料上に高い記録密度を達成しなければならないという要件によって折衷的解決を図ることができる。また、上記説明から明らかなように、このようなバイオセンサは相対的に製造コストが高いものとなる。

【０００６】薄膜トランジスタ（ＴＦＴ）は、ソーダガラスやプラスチックなどの比較的安い非シリコン基板を使用できるため相対的に製造コストが安くなる。相対的に廃棄処分が可能な材料であるため、プラスチック基板の利用により付加的利点を付与することができる。さらに、ＴＦＴは、広い面積のアレイとして容易に製造することが可能であり、このような技術は、例えばアクティブ・マトリックス型液晶表示装置の製造などにおいて産業の中ですでに広く利用されている。したがってその製造工程は十分に証明されたものであり、特にシリコン基板デバイスと比較して、相対的に低いコストで高い歩留まりの動作可能なデバイスを高い信頼性で得ることができる。シリコン基板から入手可能なアレイよりも広い面積のアレイを高い信頼性で製造できることを考慮すると、これらの利点はさらに高まる。このような広い面積のアレイ用としてシリコン・ウェーハ基板を使用することには非常に大きな問題があると考えられている。その理由として、必然的に採用しなければならない基板材料自体と半導体製造技術とに起因して、アレイの製造がますます困難となりかつコストが高くなるということが挙げられる。

【０００７】ある種の物質を検知するためにこのようなデバイスを使用する際そのデバイスの性能と関連して欠点も存在する。ＭＯＳＦＥＴには、ドープされたシリコン基板上に支持されたシリコン二酸化物（SiO_2）から成る比較的薄い層が一般に含まれる。このSiO_2層は層の厚さに逆比例する固有静電容量を有する。約１００ｎｍの典型的厚さでSiO_2層を設ける場合、デバイスから静電容量性信号のかなりの損失が生じる。この損失はSiO_2層の固有静電容量に起因するものである。非常に薄い層としてSiO_2層を設けて信号出力の改善

を図る場合、使用中デバイスが非常に不安定になる。検知用電極を非常に小型にすればこれらの設計上の矛盾の軽減が可能となる。しかし、検知用電極は、同定対象物質を受容するために使用するものであるため、実際に使用可能なサイズで検知用電極を製造する必要がある。したがってＭＯＳＦＥＴのゲート領域を比較的広くとる必要があるが、比較的広いゲート領域を設けることにより、有限サイズのシリコン基板上に収容できるトランジスタの記録密度が大幅に減少し、この減少が今度はセンサ・アレイ内に収容できるセンサ・セルの数を減らすことになるという点で、化学センサ用としてのシリコントランジスタの利用に関わる基本的な製造上の問題が生じることになる。

【０００８】特に化学センサやバイオセンサの場合、非常に高い記録密度を達成する必要性がデバイス設計時の支配的要因とはならないので、比較的安い価格で広い面積のアレイとして容易にＴＦＴの製造が可能であることは、従来使用されているシリコンデバイスと比較して著しい利点を示す。したがって、同定対象サンプルを受容するアレイの各センサ・セルに関連する領域は、必要な場合アクティブな半導体の構成要素の在る場所から移すことが可能となり、現行のシリコン基板デバイスに関して存在する絶縁という問題が多少とも解決される。さらに、同定対象サンプルを受容する検知領域（ＤＮＡセンサ用電極の形をしたものであってもよい）は、比較的広いサイズのものにすることが可能となり、検知領域が拡大され、性能の改善が図られる。さらに、これらのデバイスを使用している現在の多くのアプリケーションで見られる充填密度からＴＦＴの充填密度を減らすことが可能となり、完全に機能するデバイスの歩留まりの上昇を既存の製造工程から得ることができるという点で、この拡大された検知領域の利用によって別の利点が付与されることになる。

【０００９】ＴＦＴはシリコン基板トランジスタより低い移動度を示すことが知られており、バイオセンサの特別の利点である広い面積のアレイから成るトランジスタ・デバイスとしてＴＦＴを製造する場合、ＴＦＴはアレイ内のトランジスタ間での伝達特性の変動を示す可能性がある。アレイ・サイズが大きくなるにつれてこれらの変動は顕著になり、特に、１つのサンプルの同定を行うために一般に非常に多数のサンプルの分析が必要なＤＮＡバイオセンサの場合、広い面積のアレイはサンプル分析に必要な時間の低減に非常に意義のある利点となる。

【００１０】それ故、電極と、同定対象サンプルとの間で生じる静電容量を測定手法として利用する場合、ＴＦＴの性能の変動性と関連する潜在的欠点が解決され、センサ・セルから成る広い面積のアレイの形の化学センサ用アクティブ・デバイスとしてこのようなデバイスを容易に使用可能とすることが本発明の好適な形態としてさらに理解される。

【００１１】化学センサ用としてＴＦＴを使用することにより、シリコン基板デバイスの使用に優るコスト上の利点が得られるのみならず、改善された検知領域を持つ広い面積のアレイの製造能力も得られることになる。さらに、改善された廃棄性という有意義な付加的利点も生じる。この利点は、上述のように、このようなデバイスが廃棄処分までに１回しか使用されない可能性があるという理由で、バイオセンサ・デバイスや化学センサ・デバイスにとって特に重要な利点である。

【００１２】したがって、薄膜トランジスタを使用する改善されたセンサ・セルを提供することが本発明の目的である。さらに、同定対象サンプルを受容する電極から生じる電極での静電容量の検出を測定手法として利用すること、さらに、薄膜トランジスタの動作を制御するためにこの静電容量を利用することが本発明の目的である。

【００１３】本発明の第１の態様によれば、薄膜トランジスタと、薄膜トランジスタのゲート電極と結合された、同定対象サンプルの受容手段とを具備するセンサ・セルとが提供される。

【００１４】好適な構成では、上記センサ・セルは基準コンデンサを具備し、サンプル用電極と基準コンデンサとは薄膜トランジスタのゲート電極と結合された静電容量分割回路(capacitance divider circuit)として構成され、この分割回路は、サンプル用電極で生じた静電容量の値に従ってゲート電極へ出力される電圧パルスの振幅の制御用として設けられる。

【００１５】センサ・セルの好適な構造では、基準コンデンサは、ゲート電極と、絶縁体層によってこのゲート電極から分離された、ゲート電極の下に在る埋込み領域とを具備する。

【００１６】好適には、上記受容手段がサンプル用電極を具備し、同定対象サンプルのサンプル用電極による受容に応じてサンプル用電極において生じる静電容量値に従って薄膜トランジスタの動作を制御するように構成されることが望ましい。

【００１７】代替の構成では、センサ・セルは、導通状態と非導通状態との間で切替えを行うスイッチング・トランジスタを具備し、さらに、薄膜トランジスタにはゲート電極が含まれ、スイッチング・トランジスタが非導通状態へ切り替えられた場合、導通状態でスイッチング・トランジスタによってゲート電極へ出力される電圧の大きさが、サンプル用電極において生じる静電容量の値に従って小さくなるように構成される。

【００１８】好適には、本発明のこの第１の態様では、センサ・セルが、導通状態と非導通状態との間でスイッチング・トランジスタを切り替えるための選択用パルスを出力する選択用ラインと、薄膜トランジスタのゲート電極へ電圧を供給する書込み用ラインと、読出し(read)電圧を薄膜トランジスタへ供給する読出し用ラインとを

有し、選択用パルスをスイッチング・トランジスタへ出力することにより書込みサイクルが可能になり、この書込みサイクルによってスイッチング・トランジスタを導通状態へ切り替えて、薄膜トランジスタの制御ゲートへの電圧を供給可能とし、その場合、選択用パルスを終了させることにより読出しサイクルが可能になり、この読出しサイクルによってスイッチング・トランジスタの非導通状態への切替えを行うことにより、薄膜トランジスタのゲート電極における電圧の大きさが変化し、この変化によって薄膜トランジスタが非導通状態へ切り替えられ、薄膜トランジスタからの出力信号の供給を終了させるように構成されることが望ましい。選択用パルスの終了と、非導通状態への薄膜トランジスタの切替えとの間で要する時間はサンプル用電極における静電容量の値に依って決定される。

【００１９】好適には、センサ・セルは、フィルム・トランジスタの中を流れるプリセットレベルの電流を供給する定電流源を含む閾値電圧補償回路(threshold voltage compensation)と、この定電流源を薄膜トランジスタと選択的に結合するスイッチ手段とを含むことができることが望ましい。

【００２０】最も好適には、センサ・セルが薄膜トランジスタと結合された追加のトランジスタを具備し、電圧パルスが薄膜トランジスタのゲート電極へ出力され、定電流源が薄膜トランジスタから切断されたとき、薄膜トランジスタからの出力電流の大きさが、定電流源によって決定された第１のレベルから、サンプル用電極において生じる静電容量の値に従う第２のレベルへ変化するように構成されることが望ましい。

【００２１】好適には、薄膜トランジスタとオーバーラップしない位置に上記受容手段が構成され、薄膜トランジスタのゲート領域を覆わない位置で受容手段がサンプルを受容するような構成となることが望ましい。

【００２２】好適には、センサ・セルがプラスチック基板上に製造されることが望ましい。本発明の第２の態様によれば、本発明の第１の態様に従うセンサ・セルの行と列とから成るアレイを具備するセンサが提供される。

【００２３】本発明の第３の態様によれば、薄膜トランジスタと、サンプルを受容するサンプル用電極とを含むセンサ・セルを設けるステップと、サンプル用電極によるサンプル受容からサンプル用電極において生じる静電容量の値に従って薄膜トランジスタの動作を制御するステップとを有するサンプルの同定方法が提供される。

【００２４】好適には、上記同定方法は、基準コンデンサを設けるステップと、薄膜トランジスタのゲート電極と結合された静電容量分割回路としてこの基準コンデンサとサンプル用電極とを構成するステップと、サンプル用電極において生じる静電容量の値に従ってゲート電極へ出力される電圧パルスの振幅を制御するステップとを有することが望ましい。

【００２５】好適には、本発明の上記第２の態様では、上記方法は、導通状態と非導通状態との間の切替えを行うスイッチング・トランジスタとサンプル用電極とを結合するステップと、スイッチング・トランジスタを導通状態にして薄膜トランジスタのゲート電極へ電圧を供給するステップと、サンプル用電極をスイッチング・トランジスタと結合し、それによって、スイッチング・トランジスタが非導通状態へ切り替えられたとき、薄膜トランジスタのゲート電極へ供給される電圧の大きさがサンプル用電極において生じる静電容量の値に従って変化するステップを有することが望ましい。

【００２６】好適には、選択用ラインからスイッチング・トランジスタへ選択用パルスを出力することにより非導通状態と導通状態との間でスイッチング・トランジスタが切り替えられ、薄膜トランジスタのゲート電極へ電圧を供給するための書込み用ラインと、薄膜トランジスタへ読出し電圧を供給するための読出し用ラインとが設けられ、スイッチング・トランジスタへ選択用パルスを出力することにより書込みサイクルを可能にし、この書込みサイクルによってスイッチング・トランジスタを導通状態へ切り替え、この切替えによって、薄膜トランジスタの制御ゲートへ電圧を出力し、さらに、選択用パルスを終了させることにより読出しサイクルを可能にし、この読出しサイクルによってスイッチング・トランジスタを非導通状態へ切り替え、この切替えにより、薄膜トランジスタのゲート電極における電圧の大きさを変化させ、その変化によって薄膜トランジスタを非導通状態へ切り替え、薄膜トランジスタからの出力信号を終了させ、選択用パルスの終了と、非導通状態への薄膜トランジスタの切替えとの間で要する時間がサンプル用電極における静電容量の値に依って決定されることが望ましい。

【００２７】最も好適には、上記方法がプラスチック基板上に薄膜トランジスタを設けるステップを有することが望ましい。

【００２８】好適には、上記方法が、追加のトランジスタを薄膜トランジスタと結合し、薄膜トランジスタのゲート電極へ電圧パルスを出力し、定電流源を薄膜トランジスタから切断し、それにより、定電流源によって決定された所定の第１のレベルから、サンプル用電極において生じる静電容量の値に従って決定される第２のレベルへ、薄膜トランジスタから得られる出力電流の大きさを変えるステップも有することが望ましい。

【００２９】本発明の第４の態様によれば、本発明の第１の態様に従うセンサ・セルを具備するバイオセンサまたは本発明の第２の態様に従うセンサが提供される。

【００３０】本発明の第５の態様によれば、本発明の第１の態様に従うセンサ・セルまたは本発明の第２の態様に従うセンサを具備する指紋認識装置が提供される。

【００３１】本発明の第６の態様によれば、本発明の第

3の態様に従うバイオセンサまたは指紋認識装置の操作方法が提供される。

【００３２】図１を参照すると、化学センサなどのセンサ２は、行６、６ａ...６ｎと列８、８ａ...８ｎとで配設されるセンサ・セル４ａ、４ｂ...４ｎから成るアレイを具備する。各センサ・セル４ａには薄膜トランジスタ(TFT)Ｔ１、電極１０、さらなるトランジスタＴ６と基準コンデンサC_rとが含まれる。またセンサ２には、列プリセット・レジスタ１２と、行選択レジスタ１４と、列選択レジスタ１６と、以下に説明する作動も含まれる。別の列選択レジスタ２２の制御の下で作動する多重化／増幅回路２０が、センサ・セルからの出力信号の増幅と多重化とを行うために設けられ、出力ライン２４でセンサ・アレイから出力信号が出力される。図１では、電極１０は指先を受ける平板電極として示されているが、同様に電極１０は溶液中の電極を含むことも可能である。アレイのセンサ・セルの各々には図１に図示のセンサ・セル４ａとして構成される回路が含まれる。

【００３３】図１に図示のセンサは定常状態検出モードで作動し、トランジスタＴ１のゲート電極２６の電圧は、基準コンデンサC_rの値と組み合わされた、同定対象サンプルを受容する電極１０から結果として生じる電極１０（図１にコンデンサ記号C_sで示す）で生じる静電容量の値によって決定される。

【００３４】サイクルの開始時に、例えば列８などの列内のセンサ・セルは、列プリセット・レジスタ１２からの電圧をプリセット用ライン２８に印加することにより予め設定される。各セルのトランジスタＴ６はＯＮになり、バイアス電圧V_pがトランジスタＴ１のゲート電極２６に印加される。トランジスタＴ１がその特性曲線の所定の動作点にセットされるようにこのバイアス電圧V_pは出力され、非導通状態から導通状態への切替え準備ができる。また、以下に説明するように後続パルスがゲート電極２６に印加されたとき、ゲート電極２６の電圧があるレベルまで上昇しないことが上記切替えによって保証される。そのようなレベルとはトランジスタＴ１を通すことができないような高すぎる電流レベルであり、おそらくトランジスタＴ１を破壊することになるようなレベルの電流である。

【００３５】行選択レジスタ１４の使用により、行選択用パルスがライン３０で基準コンデンサC_rを介してノードＮへ出力される。列選択レジスタ１６の使用により、列選択用パルスがライン３２で供給される。行選択用パルスと列選択用パルスとは任意の時点に１つの行と１つの列に対してしか出力されないので、図１のセンサ・セル４ａなどの単一セルの選択が可能になる。例えば、同定の対象とする指紋を持つ指先をセンサ４ａが受けると仮定する。電極１０が指先の一部を受容し、列８ａ内のすぐ近くに隣接するセンサ・セル４ｂの電極１０ａがその指先の隣接部分を受容する。指先の表面が電極１０と１０ａとの協働電極として機能するため、指先と電極１０と１０ａの各々との間の静電容量の値（図１にC_sとして示す）の読出しが可能となる。静電容量C_sとC_rとがＡＣ分割器を実質的につくりだすため、センサ・セル４ａがライン３０で行選択用パルスを受信したとき、基準静電容量C_rの値と、電極１０に接した指先から生じる静電容量の値C_sとに従ってノードＮにおける電圧の大きさが変動する。

【００３６】上述のように、ゲート電極２６に対する電圧V_pの印加によってほとんど導通点までトランジスタＴ１にバイアスがかけられる。したがって、ライン３０に対する行選択用パルスの印加と、ライン３２に対する列選択用パルスの印加とによってセンサ・セル４ａが選択された場合、ノードＰにおける初期値V_pの電圧の大きさは静電容量の相対値C_sとC_rとによって決定される値まで上昇する。C_rが固定値コンデンサであるため、この電圧の値は静電容量の値C_sに比例するものになる。この当然の結果としてトランジスタＴ１から得られる出力電流の値は静電容量の値C_sに比例することになる。したがって、薄膜トランジスタＴ１は、同定対象サンプル（指先の指紋の一部）のサンプル用電極による受容の結果生じる、サンプル用電極１０で生じる静電容量の値に従って制御されることになる。

【００３７】出力ライン３４の電流は多重化／増幅回路２０へ送出される。多重化／増幅回路２０では、ライン３２の列選択信号と同時に、第２の列選択レジスタ２２からの選択信号がトランジスタＴ１に対して与えられる。バイアス電圧V_{bias}がトランジスタＴ５のゲート電極へ出力される。このようにして、トランジスタＴ１の適切な選択により、ライン３４の出力電流の出力部２４上へ増幅と多重化とを行うことが可能となる。同様に、他のセンサ・セルからの出力電流を出力部２４上へ多重化することも可能である。

【００３８】センサ２が指紋認識装置を具備している場合、センサと接触して置かれた指先には、或る一定のサンプル用電極と接触した指紋パターンの山部が生じ、別のサンプル用電極と接触した指紋パターンの谷部が生じる。電極１０によって指紋の山部が受容され、電極１０ａによって指紋の谷部が受容されたと仮定すると、センサ・セル４ａの静電容量の値C_sはセンサ・セル４ｂの静電容量の値C_sとは異なるものとなる。指紋パターンの山部または谷部を受容するアレイ内の他のセンサ・セルについても同じことが当てはまる。典型的には、センサ４は２００×３００のセンサ・セル・アレイを具備することができる。したがって、行選択レジスタ１４、及び、列選択レジスタ１６と２２からの信号の適切なタイミングをとることによって、アレイのセンサ・セルを連続的に走査し、出力部２４に現れるセンサ・セルの多重化された出力信号を記憶装置へ送出することが可能となる。比較器によって、これらのサンプルの格納された値

を参照値と比較することが可能となり、このような比較の結果、指紋の同定が可能となる。センサ２によって検知されるような指紋画像の表示を行うための表示部へ出力部２４の出力信号を送出することもできる。

【００３９】好適には、多重化／増幅回路２０をセンサ２と一体的に製造することが望ましく、その場合、回路のトランジスタ（その一部としてトランジスタＴ１～Ｔ５を図示）はセンサ２と共通の基板３６上にＴＦＴを具備するものであってもよい。各センサ・セル用トランジスタＴ６はＴＦＴを具備するものであってもよい。基板３６は任意の適切な支持材料を具有するものであってもよいが、好適には、センサ２から成るすべてのトランジスタをＴＦＴとして製造する場合、基板３６がプラスチック材料を含むことが望ましい。

【００４０】図１に図示の定常状態検出センサを指紋認識装置と関連して説明したが、ＤＮＡや抗体などの液状の生体材料の検出や認識を行うバイオセンサとしてこの定常状態検出センサを利用することも可能である。この場合、溶液中の物質を受容するいくつかの電極が設けられる。この物質から生じる静電容量の値を所定の参照値と比較して特定物質の同定を行うことが可能となる。

【００４１】図２は本発明に従うセンサ・セルの代替実施例を示す。図２に図示のセンサ・セルは‘変化検出(transient detection)’モードで作動し、この‘変化検出’モードで、例えば、同定の対象とするＤＮＡサンプルを受容する電極から生じる静電容量の値によって決定される時定数を利用してサンプルの同定が行われる。

【００４２】図２に図示のセンサ・セル４では、スイッチング・トランジスタＴ７が電極１０と結合され、トランジスタＴ７と電極１０との間に設けられたノードＰが薄膜トランジスタのゲート電極Ｔ１と結合される。選択用ライン４０、書込み用ライン４２及び読出し用ライン４４が、それぞれ、選択信号Ｖｓｅｌｅｃｔ、プリセット信号Ｖｐｒｅｓｅｔ及び読出し信号Ｖｒｅａｄを出力するために設けられる。出力部２４で出力信号を出力するために多重化／増幅回路２０が設けられる。

【００４３】液状のＤＮＡサンプルの同定と関連して図２に図示の回路の動作を説明する。しかし、指紋認識の場合についても図２に図示の変化検出回路は、図１を参照して説明した方法と同じ方法で利用可能であると理解すべきである。指紋検出の場合、図２の参照電極４６は指先の表面によって構成され、図２の電圧Ｖｒｅｆは指先の表面に発生する電荷によって出力されることになる。

【００４４】動作サイクルの開始時に、双方ともＴＦＴを具備することができるトランジスタＴ１とＴ７は非導通すなわちＯＦＦ状態にある。電極３０は、好適な容器内で電極として構成され、この容器の中へ液状のＤＮＡが入れられる。ＤＮＡは固定化が可能なため電極１０により受容され、その結果、静電容量値C_Aがサンプル用電極１０と参照電極４６との間に生じる。

【００４５】予め設定されたサイクルが開始され、トランジスタＴ７のゲート電極へ電圧Ｖｓｅｌｅｃｔを印加することによりスイッチング・トランジスタＴ７が非導通状態から導通状態へ切り替えられる。同時に、予め設定された電圧ＶｐｒｅｓｅｔがトランジスタＴ７のソース電極へ供給され、読出し電圧ＶｒｅａｄがトランジスタＴ１のソース電極へ印加される。トランジスタＴ７がＯＮに切り替えられると、ノードＰにおける電圧が予め設定された電圧Ｖｐｒｅｓｅｔレベルまで上昇し、ノードＰにおける電圧がトランジスタＴ１の閾値電圧を上回ると、トランジスタＴ１はＯＮに切り替わり、トランジスタＴ１の出力部の電流はノードＰ（トランジスタＴ１のゲート電極）における電圧の関数となる。

【００４６】次いで、選択電圧Ｖｓｅｌｅｃｔを終了させることにより読出しサイクルが開始され、トランジスタＴ７は元の非導通すなわちＯＦＦ状態へ切り替えられる。トランジスタＴ７がＯＦＦに切り替えられると、ノードＰの電圧はトランジスタＴ７を介する漏洩によって低下し、この漏洩が生じる速度すなわち時定数は静電容量値C_Aに依って決定され、さらに、この静電容量値はサンプル用電極１０が受容するＤＮＡサンプルの同定量に依って決定される。ノードＰにおける電圧の大きさが小さくなるにつれて、薄膜トランジスタＴ１の出力部で電流の相関的減少が生じ、この電流は多重化／増幅回路２０へ送出される。ノードＰにおける電圧がトランジスタＴ１の閾値電圧以下まで低下した場合、トランジスタＴ１はＯＦＦに切り替わり、多重化／増幅回路２０へ送出される電流をトランジスタＴ１の中を流れる漏れ電流のレベルまでさらに低下させる。トランジスタＴ７はデジタル・スイッチング・トランジスタとして使用され、一方、トランジスタＴ１はアナログ電圧から電流への変換器として機能することが上記説明から理解される。したがって、静電容量値C_Aに依って決定される電流をトランジスタＴ１の出力部でモニターすることにより、電極１０が受容するサンプルの同定量を決定することが可能となる。

【００４７】バイオセンサとして使用するために、図２に図示のようなセンサ・セルの対を設けることができる。一対の一方のセルはサンプル用セルとして機能し、対のもう一方は、反応が生じなかった参照セルとして機能する。

【００４８】化学センサまたはバイオセンサ（ＤＮＡセンサなど）として図１と図２に図示のセンサ・セルを使用する場合、同定の対象とする化学材料や生体材料をまずセルの中へ書き込み、次いで参照電極上へ書き込む必要がある。この書込みは、セルの書込みフェーズと考えることができ、デバイスの製造時に好適に行われる。インクジェット・ヘッドを都合よく使用して化学材料や生体材料の付着を行うことが可能であり、電極に電荷を印

加する電磁付着によって電極上への付着を補助して、電極の所望の付着個所へ付着物質を引きつけるようにすることができる。

【００４９】図３は、薄膜トランジスタＴ１と、電極１０と、基準コンデンサC_rとを設けるために利用可能な半導体構造の実施態様を示す図である。

【００５０】図３のＴＦＴ構造にはポリシリコン４８から成る層が含まれ、このポリシリコン層は好適にはプラスチックまたはソーダガラス材料から成る材料であることが望ましい基板３６によって支持される。ゲート電極２６は、ポリシリコン層４８上に形成され、シリコン二酸化物から成る絶縁層５０によってポリシリコン層から分離される。ゲート電極２６は不動態化層(passivation layer)５２、５４によって覆われる。

【００５１】絶縁層５０とゲート電極２６とはポリシリコン層４８の領域一帯を延在するように構成され、基板３６上に形成された金属またはドープされたポリシリコンから成る埋込み領域５６を覆う。不動態化層５２、５４には下方へ延伸する井戸が設けられ、埋込み領域５６を覆う領域でゲート電極２６の露出が行われる。金、銀あるいはプラチナを含むものであってもよい電極１０が下方へ延伸し、ゲート電極２６と接触する井戸の中に形成される。このようにして、埋込み領域５６とゲート電極２６との間に基準コンデンサが設けられる。例として図３では基準コンデンサは点線で示されている。

【００５２】また、図３に図示の構造はＴＦＴを一体化したものであって、シリコン基板トランジスタを一体化したものではないため、高価なシリコン基板材料上に最大の記録密度を達成する必要性と矛盾することなく、ＴＦＴとオーバーラップしないように電極１０の配置を行うことが可能である。その結果ＴＦＴのゲート領域を覆わないように電極１０は構成される。したがって、電極１０は、デバイス感度の改善を図ることが可能な拡大サイズの電極とすることが可能となり、さらに電極において生じるウェット環境からＴＦＴを絶縁するために必要な封入容器をより容易に、かつ、より高い信頼性で製造することが可能となる。なぜなら、デバイスの高い記録密度を高価な基板上に達成しなければならないという要件が存在しないからである。

【００５３】薄膜トランジスタＴ１と、電極１０と、基準コンデンサC_rとを一体化したコンパクトな構成がこの構造によって与えられることが図３から解る。この結果、図１の定常状態検出センサ・セルの中にこの構造を一体化することが可能となる。同定対象サンプルが電極１０によって受容されると、電極１０とサンプルとの間に生じる図３に図示の静電容量の値C_sは、必須の基準コンデンサC_rと組み合わされて、図１を参照して説明した静電容量分割回路が形成される。この分割回路によってＴＦＴの動作が制御される。

【００５４】図２に図示の変化検出センサ・セルの場合、基準コンデンサが不要なため、埋込み領域５６を省くことができる。

【００５５】上述のように、ポリシリコンＴＦＴに関する１つの問題点として閾値電圧の変動がある。この変動を補償し、ＴＦＴからの出力に匹敵する出力を広い面積の基板にわたって供給するセンサ・セルの代替回路が図４に例示されている。

【００５６】図４のセンサ・セルでは、薄膜トランジスタＴ１はスイッチＳを介して定電流源I_{source}または出力ラインのいずれかと結合される。スイッチング・トランジスタとして作動する追加トランジスタＴ８が、薄膜トランジスタＴ１のゲートとドレーン電極との間で接続され、基準コンデンサC_rがトランジスタＴ１のゲートとソース電極との間で接続される。同定対象サンプルを受容する電極（図４には図示せず）もトランジスタＴ１のゲート電極と結合される。したがって、図１を参照して説明した方法と同様の方法で、サンプル静電容量C_sによって、基準コンデンサC_rを備えた静電容量分割器が形成される。

【００５７】トランジスタＴ８がＯＮになると、トランジスタＴ１の、ゲートからソースへの電圧V_{GS}と、ドレーンからソースへの電圧V_{DS}とは等しくなる。このような条件の下で、トランジスタＴ１の動作特性は図５に示すように単純化される。スイッチＳが位置“１”にあるとき、定電流源I_{source}からの電流がトランジスタＴ１を介して引かれ、トランジスタＴ１の両端にわたる電圧降下V_{DSref}という結果が生じる。トランジスタＴ８がＯＮになっている（したがってトランジスタＴ１の場合V_{GS}はV_{DS}に等しい）ため、トランジスタＴ１の両端にわたって生じる電圧降下V_{DSref}は基準コンデンサC_rの中に蓄えられる。

【００５８】薄膜トランジスタＴ１における閾値変動は、図６に図示のように、（V_{GS}がV_{DS}に等しい場合）トランジスタＴ１の単純化された動作特性曲線のシフトという結果を生じる可能性もある。トランジスタＴ１の中を流れる電流の値は定電流源、I_{source}から供給されているので一定である。したがっていずれの閾値変動の場合にも、トランジスタＴ１の電源とドレーン電極との間で生じる電圧降下V_{DSref}の変化という結果を生じることになる。電圧V_{DSref}は基準コンデンサC_rの中に蓄えられる。したがって、トランジスタＴ１のゲート電極とソース電極との間の電圧V_{GS}はこの値に予め充電される。このようにして、トランジスタＴ１はその特性曲線の所定の動作点にプリセットされる。

【００５９】次に、スイッチＳは位置“２”へ動かされ、Ｔ８がＯＦＦに切り替えられた場合、出力ラインの電流I_{out}は、ノードＰにおける電圧によって支配されるので、最初、定電流源I_{source}からの電流に等しくなるが、次いで、基準コンデンサC_rに格納され

た電圧によって支配される。次いで電圧源V_{ref}がパルス出力を行った場合、ノードPにおける電圧が上昇し、電圧V_{ref}に応じてパルスが出力される。出力ラインの電流I_{out}もノードPの電圧の上昇に応じてパルスを出力する。

【0060】基準コンデンサC_rと静電容量C_sとによって容量分割器が形成されるため、電圧源V_{ref}がパルスを出力する場合のノードPにおける電圧の上昇はC_rとC_sの相対的静電容量値によって決定される。定電流源I_{source}からの電流に等しい出力電流の初期値からの出力電流I_{out}の上昇を測定して、サンプル用電極が受容したサンプルを示す静電容量の値C_sの定量化を行うことができる。

【0061】基板36上の薄膜トランジスタのような半導体素子によるスイッチ手段によってスイッチSを設けてもよいことが理解できる。

【0062】図7は、このセンサをpHセンサとして使用できる本発明の別の実施例を例示する。図7に図示の構造は図3に図示の構造と非常に類似しているため、可能なかぎり同様の参照番号を用いてこの構造の同様部分を示すことにする。

【0063】図7に図示の構造では、不動態化層52に井戸58が設けられ、ゲート電極26の露出が行われる。不動態化層54が、不動態化層52とゲート電極26上にわたって延在する連続層として井戸58の中へ設けられ、ゲート電極上にわたって、不動態化材料60から成る比較的薄い層が設けられる。尿素やグルコースなどの溶液の形で同定が行われる対象サンプルが井戸58の中へ入れられ、層60と接触して、溶液中のイオンが層60に近づき、図7で+記号によって示されるプロトンが層60の表面62に吸収される。層60は非常に薄いので、この電荷はゲート電極60へ移動し、その結果、ゲート電極26、ポリシリコン領域48及びシリコン二酸化物層50によって構成されるTFTトランジスタの動作を制御する電圧が出力される。表面62上へのイオンの吸着によって層60の中につくり出された電荷は井戸58の中へ付着した溶液のpHに関連する。したがって、TFTからの出力をモニターすることにより、溶液中の物質の同定を行うことが可能となる。

【0064】上記の説明は単なる例として行われたものであり、本発明の範囲から逸脱することなく修正を行うことが可能であることは当業者が理解するところであろう。

【0065】例として、液状の化学材料や生体材料の検出と関連してセンサ・セルについて説明を行った。しかし、センサ・セルを利用して気体などの液体以外の流体を分析することも可能であると理解すべきである。

【0066】さらに、特定の化学材料や生体材料サンプルの分析に使用する1つのセンサ・セルと関連して本発明を説明した。しかし、TFTは、シリコン基板デバイスと比較して、高い信頼性で、非常に広い面積のアレイに製造することができるので、センサを構成するセンサ・セルの行列に、参照電極上へ書き込まれた特定のDNA列を各々が持ついくつかのセンサ・セルを設けることができる。アレイの両端にわたって離間して配置された関係でこのようなセルが設けられている場合、参照電極上へ書き込まれる、DNA列などの共通の対照標準物質を持つこれらのセンサ・セルから得られる出力信号が適切な回路構成によって平均化され、高い分析精度を生むことが可能となる。TFTを用いてこの分析回路構成を基板上に製造してもよい。このようにして、本質的に、各々が共通のDNA文字列を同定するように構成されるいくつかの‘複製’センサ・セルをセンサに設けることが可能となる。TFTを利用して以上のことが可能となるのは、非常に多数のセンサ・セルを非常に広い面積のアレイの中に一体化することが可能であるためである。

【図面の簡単な説明】

【図1】本発明の第1の実施例に従うセンサを例示する。

【図2】本発明の第2の実施例に従うセンサを例示する。

【図3】図1に図示のセンサで利用するセンサ・セルの構造を例示する。

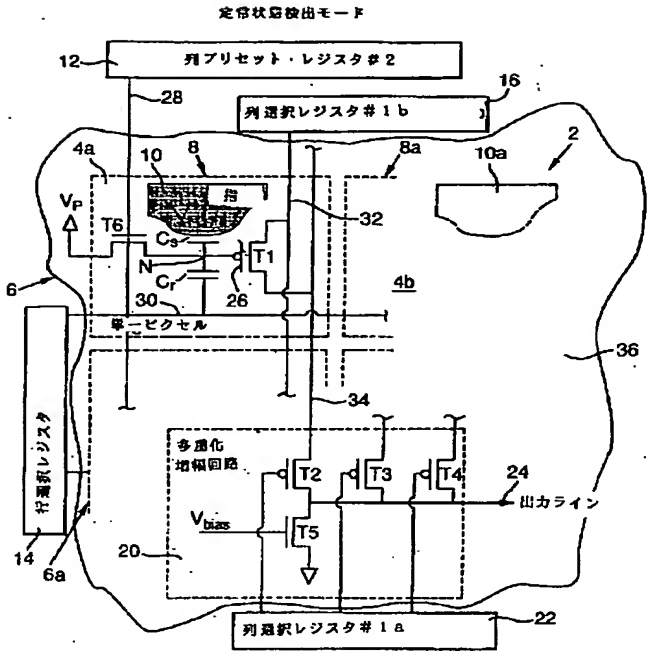
【図4】図1に図示のセンサで使用する閾値電圧の変動を含むセンサ・セルを例示する。

【図5】図4に図示のセンサ・セルの薄膜トランジスタの単純化された動作特性を例示する。

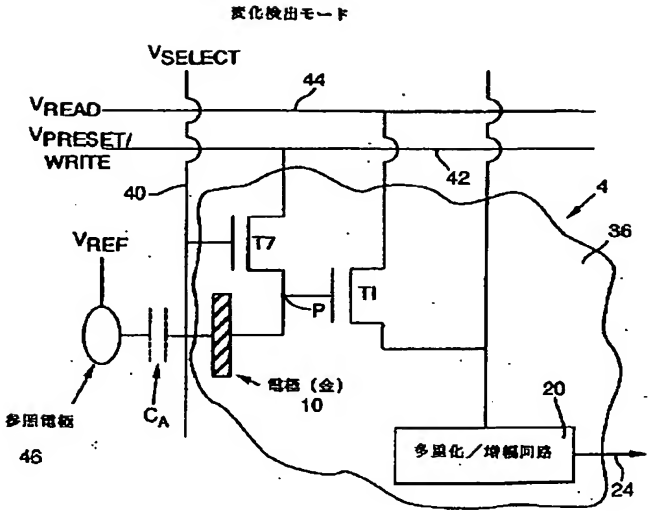
【図6】薄膜トランジスタの閾値電圧が変動する、図5に図示の単純化された動作特性の変動を例示する。

【図7】本発明に従うpHセンサとして使用されるセンサ・セルの代替構造を例示する。

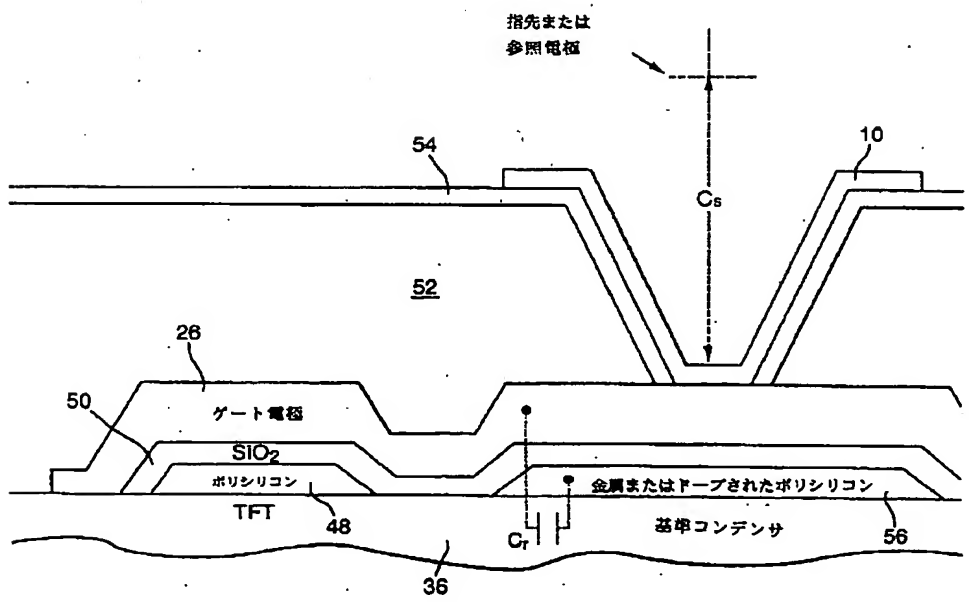
【図１】


定常状態検出モード
12
列プリセット・レジスタ＃２
28
16
列選択レジスタ＃１ｂ
2
4a
10
8
8a
10a
V_P
T6
C_S
32
N
C_T
T1
6
30
26
4b
単一ピクセル
36
34
行選択レジスタ
多重化
増幅回路
T2
T3
T4
24
出力ライン
V_{bias}
T5
20
14
6a
列選択レジスタ＃１ａ
22

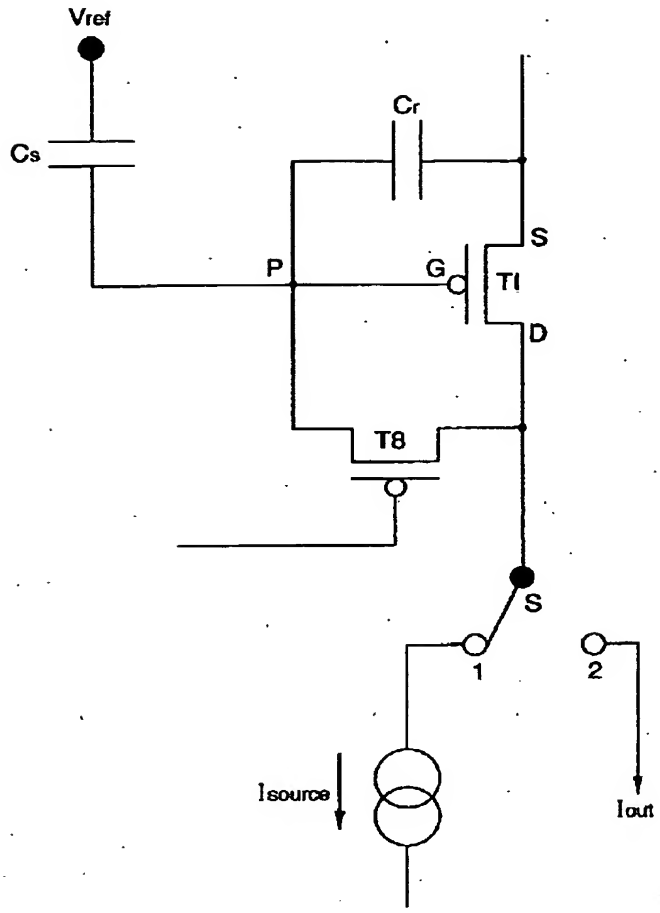
【図２】


変化検出モード
V_{SELECT}
44
V_{READ}
$V_{PRESET/}$
WRITE
42
40
4
36
V_{REF}
T7
T1
P
電極（金）
10
参照電極
46
C_A
20
多重化／増幅回路
24

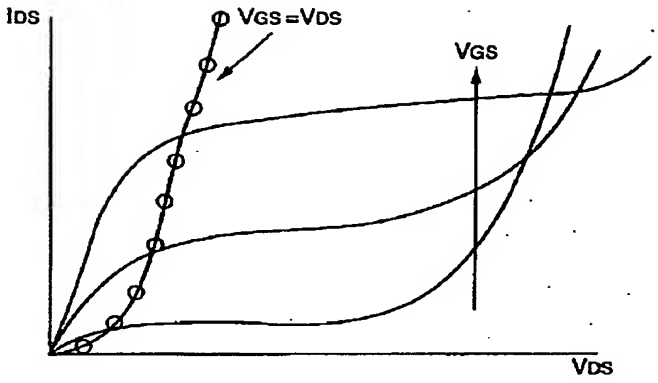
【図３】


指先または
参照電極
54
10
C_S
52
26
50
ゲート電極
SiO_2
ポリシリコン
TFT
48
金属またはドープされたポリシリコン
C_T
基準コンデンサ
56
36

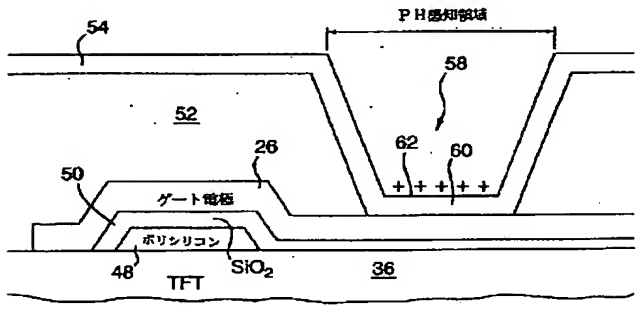
【図４】


Vref
Cs
Cr
S
P
G
TI
D
T8
S
1
2
Isource
Iout

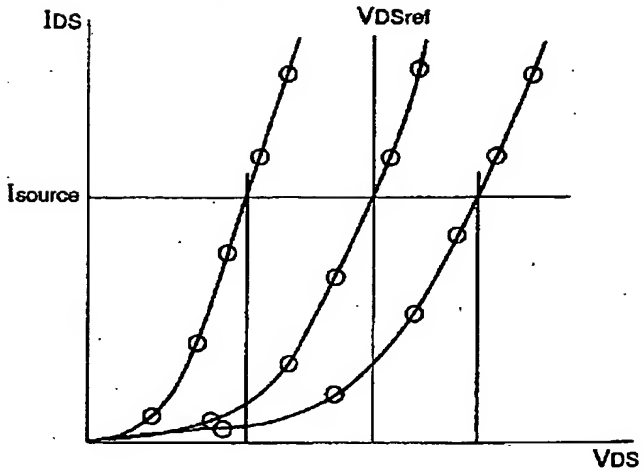
【図５】


IDS
VGS=VDS
VGS
VDS

【図７】


54
58
52
62
60
26
50
48
TFT
36

【図６】


IDS
VDSref
Isource
VDS

フロントページの続き

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Ｆターム(参考)　5F110 BB09 CC01 DD01 DD02 EE09 FF02 GG02 GG13 NN72

【外国語明細書】

1.Title of the Invention

Sensor Cell

2.Claims

1. A sensor cell comprising a thin film transistor and receiving means coupled to a gate electrode of the thin film transistor for receiving a sample for identification.

2. A sensor cell as claimed in claim 1, wherein the receiving means comprises a sample electrode, the arrangement being such that operation of the thin film transistor is controlled in dependence upon a value of capacitance arising at the sample electrode in response to receipt by the sample electrode of the sample for identification.

3. A sensor cell as claimed in claim 2, comprising a reference capacitor and wherein the sample electrode and the reference capacitor are arranged as a capacitance divider circuit coupled to the gate electrode of the thin film transistor for controlling the amplitude of a voltage pulse provided to the gate electrode in dependence upon the value of capacitance arising at the sample electrode.

4. A sensor cell as claimed in claim 3, wherein the reference capacitor comprises the gate electrode and a buried region underlying a metal layer extending into contact with the gate electrode and separated from the metal layer by an insulator layer.

5. A sensor cell as claimed in claim 4, wherein the buried region compr

ises metal or doped polysilicon.

6. A sensor cell as claimed in any one of claims 3 to 5 comprising a further transistor for affording the voltage pulse to the gate electrode of the thin film transistor in response to a select pulse afforded to the further transistor.

7. A sensor cell as claimed in claim 6, wherein the further transistor comprises a thin film transistor.

8. A sensor cell as claimed in claim 2 comprising a switching transistor for switching between a conducting condition and a non-conducting condition, the arrangement being such that a voltage provided to the gate electrode of the thin film transistor with the switching transistor in the conducting condition changes in magnitude in dependence upon the value of the capacitance arising at the sample electrode when the switching transistor is switched to the non-conducting condition.

9. A sensor cell as claimed in claim 8 comprising a select line for providing a select pulse to a gate electrode of the switching transistor for switching the switching transistor between the conducting and non-conducting conditions.

10. A sensor cell as claimed in claim 9 comprising a preset line for providing the voltage to the gate electrode of the thin film transistor and a read line for providing a read voltage to the thin film transistor. the arrangement being such that a preset cycle is enabled by providing the select pulse to the switching transistor, thereby to switch the switching transistor to a conducting condition to enable the voltage to be pr

ovided to the gate electrode of the thin film transistor, and wherein a read cycle is enabled by terminating the select pulse thereby to switch the switching transistor to the non-conducting condition, whereby the voltage at the gate electrode of the thin film transistor changes in magnitude, thereby to switch the thin film transistor to a non-conducting condition, the time taken between termination of the select pulse and switching of the thin film transistor to the non-conducting condition being dependent upon the value of capacitance at the sample electrode.

11. A sensor cell as claimed in any one of claims 3 to 7, comprising a threshold voltage compensation circuit including a constant current source for providing a preset level of current through the thin film transistor and switching means for selectively coupling the constant current source to the thin film transistor.

12. A sensor cell as claimed in claim 11 comprising an additional transistor coupled to the thin film transistor, the arrangement being such that when the voltage pulse is provided to the gate electrode of the thin film transistor and the constant current source is decoupled from the thin film transistor, the magnitude of an output current from the thin film transistor will change from a first level determined by the constant current source to a second level dependent upon the value of capacitance arising at the sample electrode.

13. A sensor cell as claimed in claim 12 comprising means for determining the change between the first and second levels of the output current from the thin film transistor.

14. A sensor cell as claimed in any one of claims 11 to 13, wherein the

switching means comprises a thin film transistor switching circuit.

15. A sensor cell as claimed in any one of the preceding claims, wherein the receiving means comprises gold, silver or platinum.

16. A sensor cell as claimed in anyone of the preceding claims, wherein the receiving means is arranged in a position offset from the thin film transistor, the arrangement being such that the sample is received by the receiving means in a position which does not overlie a gate region of the thin film transistor.

17. A sensor cell as claimed in claim 1 or 2, wherein the receiving means comprises a well portion arranged in a passivation layer overlying the thin film transistor thereby to provide a layer of passivation material overlying a metal layer extending into contact with the gate electrode, the layer of passivation material having a thickness such that an electric charge arising in the well portion from receipt by the well portion of the sample for identification creates a voltage at the gate electrode of the thin film transistor indicative of the sample.

18. A sensor cell as claimed in any one of the preceding claims, wherein the sensor cell comprises a plastics or glass substrate.

19. A sensor comprising an array of rows and columns of sensor cells as claimed in any one of the preceding claims.

20. A sensor as claimed in claim 19 comprising a row select register for selecting the rows of sensor cells of the array and a column select register for selecting the columns of sensor cells of the array.

21. A sensor as claimed in claim 19 or 20 comprising amplification means for amplifying output signals from the sensor cells.

22. A sensor as claimed in any one of claims 19 to 21 comprising multiplexing means for multiplexing output signals from the sensor cells.

23. A sensor as claimed in any one of claims 19 to 22 comprising storage means for storing reference values indicative of reference samples, comparator means for comparing the reference values with output signals from sensor cells and display means arranged to indicate whether a sample for identification matches a reference sample.

24. A sensor as claimed in any one of claims 19 to 23, wherein each sensor cell comprises a reference electrode, and wherein a plurality of reference electrodes disposed in spaced relationship throughout the array are arranged to carry a common reference substance, and the sensor further comprises circuit means for receiving and averaging output signals from those sensor cells including one of the plurality of reference electrodes carrying the common reference substance.

25. A method for identifying a sample comprising providing a sensor cell including a thin film transistor and receiving means coupled to a gate electrode of the thin film transistor for receiving the sample.

26. A method as claimed in claim 25, comprising providing the receiving means in a position offset from the thin film transistor such that the sample is received by the receiving means in a position which does not overlie a gate region of the thin film transistor.

27. A method as claimed in claim 25 or 26, comprising providing the rec eiving means as a sample electrode and wherein the operation of the thin film transistor is controlled in dependence upon a value of capacitance arising at the sample electrode in response to receipt by the sample el ectrode of the sample.

28. A method as claimed in claim 27 comprising providing a reference ca pacitor and arranging the reference capacitor and the sample electrode a s a capacitance divider circuit coupled to the gate electrode of the thi n film transistor, and controlling the amplitude of a voltage pulse prov ided to the gate electrode in dependence upon the value of capacitance a rising at the sample electrode.

29. A method as claimed in claim 28 comprising providing the reference capacitor as a buried region underlying a metal layer extending into con tact with the gate electrode and separated from the metal layer by an in sulator layer.

30. A method as claimed in claim 29 comprising providing the buried reg ion as a region of metal or doped polysilicon.

31. A method as claimed in claim 28 comprising providing a further tran sistor and controlling the voltage pulse provided to the gate electrode by applying a select pulse to the further transistor.

32. A method as claimed in claim 31 comprising supplying the further tr ansistor as a thin film transistor.

33. A method as claimed in claim 27 comprising coupling the sample electrode with a switching transistor for switching between a conducting condition and a non-conducting condition, providing a voltage to the gate electrode of the thin film transistor with the switching transistor in the conducting condition, and coupling the sample electrode to the switching transistor, whereby when the switching transistor is switched to the non-conducting condition the voltage provided to the gate electrode of the thin film transistor changes in magnitude in dependence upon the value of the capacitance arising at the sample electrode.

34. A method as claimed in claim 33, wherein the switching transistor is switched between the non-conducting and conducting conditions by providing a select pulse from a select line to the switching transistor.

35. A method as claimed in claim 34 comprising providing a preset line for providing the voltage to the gate electrode of the thin film transistor, a read line for providing a read voltage to the thin film transistor, enabling a preset cycle by providing the select pulse to the switching transistor, thereby to switch the switching transistor to a conducting condition to provide the voltage to the gate electrode of the thin film transistor, and enabling a read cycle by terminating the select pulse thereby to switch the switching transistor to the non-conducting condition, whereby the voltage at the gate electrode of the thin film transistor changes in magnitude, thereby to switch the thin film transistor to a non-conducting condition, the time taken between the termination of the select pulse and switching of the thin film transistor to the non-conducting condition being dependent upon the value of capacitance at the sample electrode.

36. A method as claimed in any one of claims 28 to 30 comprising providing a threshold voltage compensation circuit including a constant current source for providing a preset level of current through the thin film transistor, and switching means for selectively coupling the constant current source to the thin film transistor.

37. A method as claimed in claim 36 comprising coupling an additional transistor to the thin film transistor, providing the voltage pulse to the gate electrode of the thin film transistor and decoupling the constant current source from the thin film transistor thereby to change the magnitude of the output current from the thin film transistor from a first level determined by the constant current source to a second level dependent upon the value of capacitance arising at the sample electrode.

38. A method as claimed in claims 25 or 26, wherein the receiving means is provided as a well portion arranged in a passivation layer overlying the thin film transistor so as to provide a layer of passivation material overlying a metal layer extending into contact with the gate electrode, the layer passivation material having a thickness such that an electric charge arising in the well portion from receipt by the well portion of the sample for identification creates a voltage at the gate electrode of the thin film transistor indicative of the sample.

39. A method as claimed in any one of claims 25 to 37, comprising fabricating the sensor cell on a plastics or a glass substrate.

40. A method as claimed in any one of claims 25 to 38 comprising providing a plurality of sensor cells arranged as an array of rows and columns of sensor cells.

41. A method as claimed in claim 40 comprising providing a row select register for selecting the rows of sensor cells in the array and a column select register for selecting the columns of sensor cells of the array.

42. A method as claimed in claim 40 or 41 comprising providing amplification means for amplifying output signals from the sensor cells.

43. A method as claimed in any one of claims 40 to 42 comprising providing multiplexing means for multiplexing output signals from the sensor cells.

44. A chemical sensor comprising a sensor cell as claimed in any one of claims 1 to 18 or a sensor as claimed in any one of claims 19 to 24.

45. Fingerprint recognition apparatus comprising a sensor cell as claimed in any one of claims 1 to 18 or a sensor as claimed in any one of claims 19 to 24.

46. A method of operating a biosensor comprising a method as claimed in any one of claims 25 to 43.

47. A method of operating fingerprint recognition apparatus comprising a method as claimed in any one of claims 25 to 43.

3. Detailed Description of Invention

The present invention relates to sensor cells and to sensors which incorporate such sensor cells.

Chemical sensors incorporating arrays of sensor cells including semiconductor transistors are known. Such sensors have typically used a silicon wafer as the substrate material. However, silicon is a relatively expensive material. Furthermore, for certain types of sensors, such as biosensors, disposability of the sensor after use is an especially important issue as the biosensor can only be used once before disposal. When silicon is used as the substrate material, disposing of the used biosensors becomes more problematical.

Additionally, the difficulties associated with fabricating transistor arrays on silicon substrates are known to increase significantly with increase in the size of the array. Hence, with silicon substrates the tendency is for a high density of devices for any given size of array. For biosensors, this high packing density can be problematical because for many applications the active parts of the microelectronic chip incorporating the array must operate in a wet environment.

Many forms of chemical sensors, such as biosensors, have been proposed. One type of multi-biosensor comprises a pH sensor in the form of an array of four Ion Sensitive Field Effect Transistors (ISFET's) in combination with four Metal Oxide Silicon Field Effect Transistors (MOSFET's) acting as source follower circuits. However, in order to provide sufficient isolation between the ISFET's, the proposed array was relatively bulky in size. Furthermore, an IFSET is a form of transistor and considerable problems arise in isolating such devices from a solution being tested. To alleviate the problems of isolation, the ISFET's and MOSFET's have been proposed to be fabricated on a silicon layer in the form of a number of discrete sites supported on a sapphire substrate. Sapphire was used as the substrate material because of its excellent electrical isolation properties. A protectional membrane was then formed over the gate surfaces of the ISFET's, followed by membranes respectively sensitive to th

e compounds to be tested. The individual sensors so produced functioned as pH sensors and could be used to detect urea, glucose and potassium. However, as mentioned above, the sensor array was of relatively large size, measuring approximately 2mm in width and 6mm in length for a four sensor array. Furthermore, sapphire substrates can only be used to fabricate arrays to a certain size and it is well known that the concerns relating to the fabrication of arrays using silicon increase significantly with increase of array size. Additionally, the silicon and, in particular, the sapphire substrate materials are relatively expensive and therefore chemical sensors of the above type are extremely costly to fabricate. This cost aspect is particularly burdensome when considering that many types of sensors can only be used once before disposal. Moreover, these materials are not readily disposable, giving rise to significant environmental concerns regarding disposal after use.

More recently, sub-micron CMOS technology has been proposed for use as a biosensor array for DNA analysis. This technology has enabled an array of up to about 1000 sensor cells to be fabricated on a substrate having a size in the order of a few millimetres square. However, as the CMOS devices are fabricated on a silicon substrate, the proposed array has a high packing density. To isolate the active CMOS devices from the wet operating environment, a specific integrated reaction test chamber is provided in the form of a cavity arranged between two superimposed and hermetically sealed printed circuits. The DNA material to be analysed is separated into its two strands by heating and, using a biochemical process, the strands are labelled with a fluorescent molecule. An analyte containing the DNA strands is then placed in contact with the chip. If a DNA strand has a sequence matching that of a target arranged on an electrode of the sensor, hybridisation occurs which results in a physical localisation of the DNA sample onto the appropriate electrode of the chip.

The chip is then rinsed and the sensor is read with a CCD camera. As the DNA strands have been labelled with a fluorescent molecule, relative brightness on the electrodes of the device indicates where bonding has occurred. Key issues in the applicability of such devices are recognised as materials compatibility, manufacturing and packaging in order to reliably deliver a wet-chip concept and these can be compromised by the requirement to achieve a high packaging density on the silicon substrate material. Also, as will be apparent from the above description, such biosensors are relatively expensive to manufacture.

Thin film transistors (TFT's) are relatively inexpensive to manufacture as relatively cheap non-silicon substrates such as soda glass or plastic can be used. The use of a plastics substrate can provide additional benefits as it is a relatively disposable material. Furthermore, TFT's can be readily fabricated as large area arrays and such technology has already found widspread application in industry, such as for example, in the manufacture of active matrix liquid crystal display devices. The manufacturing processes are therefore well proven and a high yield of operable devices can reliably be obtained at relatively low costs, especially in comparison to silicon substrate devices. These advantages are further enhanced when considering that arrays larger than those available from silicon substrates can also be reliably fabricated. The use of silicon wafer substrates for such large area arrays is considered to be extremely problematical as it becomes increasingly difficult and expensive to fabricate the arrays in view of the substrate material itself and the semiconductor fabrication techniques which must necessarily be employed.

There are also drawbacks associated with the performance of such devices when used to sense certain substances. MOSFET's typically comprise a relatively thin layer of silicon dioxide (SiO_2) supported on a doped silicon substrate. The SiO_2 layer has inherent capacitance which is inve

rsely proportional to the thickness of the layer. If the SiO_2 layer is fabricated to a typical thickness of about 100nm, there is significant l oss of capacitive signal from the device which is due to the inherent ca pacitance of the SiO_2 layer. If the SiO_2 layer is fabricated as a very thin layer to improve signal output, the devices become very unstable in use. These design conflicts can be alleviated if the sensing electrode is made very small. However, the sensing electrode must be fabrica ted to a practical size as it is used to receive the substance being ide ntified. The MOSFET gate area must therefore be made relatively large b ut this gives rise to the basic fabrication concern regarding the use of silicon transistors for chemical sensors in that the provision of relat ively large gate areas significantly reduces the packing density of the transistors which can be accommodated on the finite size silicon substra tes, which in turn reduces the number of sensor cells that can be accomm odated in the sensor array.

For chemical or biosensors in particular, the ability of TFT's to be r eadily fabricated as large area arrays at relatively low cost presents s ignificant advantages in comparison to the conventionally used silicon d evices as the need to achieve a very high packing density is not a domin ant factor in device design. Hence, the area associated with each senso r cell of an array which receives the sample to be identified can, if ne cessary, be displaced from the active semiconductor components, alleviat ing the isolation concerns which exist with the current silicon substrat e devices. Furthermore, the sensing areas for receiving a sample to be identified, which may be in the form of electrodes for a DNA sensor, can be made relatively large in size, enlarging the sensing area and enhanc ing device performance. Additionally, the use of enlarged sensing areas can provide a further benefit in that the packing density of the TFT's can be reduced from that found in many current applications where these

devices are used providing increased yields of fully functional devices from the existing fabrication processes.

TFT's are known to exhibit lower mobility than silicon substrate transistors and, when fabricated as a large array of transister devices, which would be of particular benefit for a biosensor, TFT's can exhibit variations in transfer characteristic between the transistors in the array. These variations can become more pronounced as the array size is increased and for DNA biosensors in particular, where typically a very large number of samples need to be analysed to identify a sample, a large area array is of very significant benefit in reducing the time required to analyse samples.

Hence, it has been further realised with a preferred form of the present invention that, if the capacitance arising between an electrode and a sample to be identified is used as a measurement technique, the potential drawbacks associated with the variability in TFT performance can be overcome, enabling such devices to be readily used as the active devices for a chemical sensor in the form of a large array of sensor cells.

The use of TFT's for chemical sensors not only provides the cost benefit over the use of silicon substrate devices but also provides the ability to fabricate large area arrays with enhanced sensing areas. Furthermore, there is also the significant additional benefit of improved disposability, which is particularly important for biosensor or chemical sensor devices because, as stated above, such devices can usually be used once only before disposal.

It is therefore an object of the present invention to provide an improved sensor cell utilising thin film transistors. Furthermore, it is also an object of the present invention in which detection of the capacitance on an electrode arising from the electrode receiving a sample for identification is used as the measurement technique and this capacitance is

used to control the operation of the thin film transistors.

According to a first aspect of the present invention, there is provided a sensor cell comprising a thin film transistor and receiving means coupled to a gate electrode of the thin film transistor for receiving a sample for identification.

In a preferred arrangement, the sensor cell comprises a reference capacitor and the sample electrode and the reference capacitor are arranged as a capacitance divider circuit coupled to a gate electrode of the thin film transistor for controlling the amplitude of a voltage pulse provided to the gate electrode in dependence upon the value of capacitance arising at the sample electrode.

In an advantageous structure for the sensor cell, the reference capacitor comprises the gate electrode and a buried region underlying the gate electrode and separated therefrom by an insulator layer.

Preferably, the receiving means comprises a sample electrode, the arrangement being such that operation of the thin film transistor is controlled in dependence upon a value of capacitance arising at the sample electrode in response to receipt by the sample electrode of the sample for identification.

In an alternative arrangement, the sensor cell comprises a switching transistor for switching between a conducting condition and a non-conducting condition and wherein the thin film transistor includes a gate electrode, the arrangement being such that a voltage provided to the gate electrode with the switching transistor in the conducting condition reduces in magnitude in dependence upon the value of the capacitance arising at the sample electrode when the switching transistor is switched to the non-conducting condition.

Preferably, in this first aspect of the present invention, the sensor cell comprises a select line for providing a select pulse for switching

the switching transistor between the conducting and non-conducting conditions and a write line for providing the voltage to the gate electrode of the thin film transistor, a read line for providing a read voltage to the thin film transistor, the arrangement being such that a write cycle is enabled by providing the select pulse to the switching transistor, thereby to switch the switching transistor to a conducting condition to enable the voltage to be provided to the control gate of the thin film transistor, and wherein a read cycle is enabled by terminating the select pulse thereby to switch the switching transistor to the non-conducting condition, whereby the voltage at the gate electrode of the thin film transistor changes in magnitude, thereby to switch the thin film transistor to a non-conducting condition for terminating the provision of an output signal from the thin film transistor, the time taken between termination of the select pulse and switching of the thin film transistor to the non-conducting condition being dependent upon the value of capacitance at the sample electrode.

Advantageously, the sensor cell may include a threshold voltage compensation circuit including a constant current source for providing a preset level of current through the film transistor and switching means for selectively coupling the constant current source to the thin film transistor.

Most advantageously, the sensor cell comprises an additional transistor coupled to the thin film transistor, the arrangement being such that when the voltage pulse is provided to the gate electrode of the thin film transistor and the constant current source is decoupled from the thin film transistor, the magnitude of the output current from the thin film transistor will change from a first level determined by the constant current source to a second level in dependence upon the value of capacitance arising at the sample electrode.

Advantageously, the receiving means is arranged in a position offset from the thin film transistor, the arrangement being such that the sample is received by the receiving means in a position which does not overlie the gate region of the thin film transistor.

Preferably, the sensor cell is fabricated on a plastics substrate.

According to a second aspect of the present invention there is provided a sensor comprising an array of rows and columns of sensor cells in accordance with the first aspect of the present invention.

According to a third aspect of the present invention there is provided a method for identifying a sample comprising providing a sensor cell including a thin film transistor and a sample electrode for receiving the sample and controlling the operation of the thin film transistor in dependence upon a value of capacitance arising at the sample electrode from receipt by the sample electrode of the sample.

Preferably, the method comprises providing a reference capacitor and arranging the reference capacitor and the sample electrode as a capacitance divider circuit coupled to the gate electrode of the thin film transistor and controlling the amplitude of a voltage pulse afforded to the gate electrode in dependence upon the value of capacitance arising at the sample electrode.

Advantageously, in this second aspect of the present invention the method comprises coupling the sample electrode with a switching transistor for switching between a conducting condition and a non-conducting condition, providing a voltage to a gate electrode of the thin film transistor with the switching transistor in the conducting condition, and coupling the sample electrode to the switching transistor whereby when the switching transistor is switched to the non-conducting condition the voltage provided to the gate electrode of the thin film transistor changes in magnitude in dependence upon the value of the capacitance arising at the s

ample electrode.

Preferably, the switching transistor is switched between the non-conducting and conducting conditions by providing a select pulse from a select line to the switching transistor and a write line is provided for providing the voltage to the gate electrode of the thin film transistor, a read line for providing a read voltage to the thin film transistor, enabling a write cycle by providing the select pulse to the switching transistor, thereby to switch the switching transistor to a conducting condition to provide the voltage to the control gate of the thin film transistor, and enabling a read cycle by terminating the select pulse thereby to switch the switching transistor to the non-conducting condition, whereby the voltage at the gate electrode of the thin film transistor changes in magnitude, thereby to switch the thin film transistor to a non-conducting condition and terminate an output signal from the thin film transistor, the time taken between the termination of the select pulse and switching of the thin film transistor to the non-conducting condition being dependent upon the value of capacitance at the sample electrode.

Most preferably, the method comprises providing the thin film transistor on a plastics substrate.

Advantageously, the method also comprises coupling an additional transistor to the thin film transistor, providing the voltage pulse to the gate electrode of the thin film transistor and decoupling the constant current source from the thin film transistor thereby to change the magnitude of the output current from the thin film transistor from a first level determined by the constant current source to a second level in dependence upon the value of capacitance arising at the sample electrode.

According to a fourth aspect of the present invention, there is provided a biosensor comprising a sensor cell according to the first aspect of the present invention or a sensor according to the second aspect of the

present invention.

According to a fifth aspect of the present invention, there is provided fingerprint recognition apparatus comprising a sensor cell according to the first aspect of the present invention or a sensor according to the second aspect of the present invention.

According to a sixth aspect of the present invention, there is provided a method of operating a biosensor or fingerprint recognition apparatus according to the third aspect of the present invention.

Referring to Figure 1, a sensor 2, such as a chemical sensor, comprises an array of sensor cells 4a, 4b...4o, arranged in rows 6, 6a...6n and columns 8, 8a...8n. Each sensor cell 4a includes a thin film transistor (TFT), T1, an electrode 10, a further transistor T6 and a reference capacitor Cr. The sensor 2 also includes a column preset register 12, a row select register 14, and a column select register 16, the function of which is described below. Multiplex and amplification circuit 20, operating under the control of a second column select register 22, is also provided for amplifying and multiplexing output signals from the sensor cells to provide an output signal from the sensor array on output line 24.

In Figure 1, the electrode 10 is shown as a plate electrode for receiving a finger tip, but, equally, the electrode 10 could comprise an electrode in solution. Each of the sensor cells of the array has a circuit configured as the sensor cell 4a shown in Figure 1.

The sensor shown in Figure 1 operates in a steady state detection mode with the voltage on the gate electrode 26 of transistor T1 being determined by the value of the capacitance arising on the electrode 10 (denoted by the capacitor symbol Cs in Figure 1) resulting from the electrode 10 receiving a sample for identification, in combination with the value of the reference capacitor Cr.

At the start of a cycle, the sensor cells in a column, for example col

umn 8, are preset by the application of a voltage from the column preset register 12 on preset line 28. The transistor T6 of each cell is turned ON and a bias voltage Vp is applied to the gate electrode 26 of transistor T1. The bias voltage Vp is provided so that transistor T1 is set to a known operating point on its characteristic and is ready to switch from a non-conducting to a conducting condition. It also ensures that the voltage at the gate electrode 26, when a subsequent pulse is applied thereto, as is described below, does not rise to a level which would cause too high a current to be passed by transistor T1, possibly destroying transistor T1.

The row select register 14 is used to provide row select pulses on line 30 to the node N via the reference capacitor Cr. The column select register 16 is used to supply a column select pulse on line 32. The row select and column select pulses are only supplied to one row and one column at any point in time, enabling a single cell, such as the sensor cell 4a in

Figure 1, to be selected. Assuming, for example, that a fingertip whose fingerprint is to be identified is being received by the sensor 4a. A part of the fingertip will be received by the electrode 10 and an adjacent part of the fingertip will be received by electrode 10a of the immediately adjacent sensor cell 4b in column 8a. The fingertip surface acts a co-operating electrode to the electrodes 10 and 10a, and hence a value of capacitance, denoted as Cs in Figure 1, can be read between the fingertip and each of the electrodes 10 and 10a. The capacitances Cs and Cr create in effect an AC potential divider and hence, when the sensor cell 4a receives the row select pulse on line 30, the magnitude of the voltage at node N will vary in dependence upon the value of the reference capacitance Cr and the value of the capacitance Cs arising from the fingertip on the electrode 10.

As stated above, transistor T1 is biased almost to the point of conduction by the application of the voltage Vp to the gate electrode 26. Hence, when the sensor cell 4a is selected by the application of a row select pulse on line 30 and a column select pulse on line 32, the magnitude of the voltage at node P, initially at value Vp, will increase to a value determined by the relative values of the capacitances Cs and Cr. Because Cr is a fixed reference value capacitor, the value of this voltage will be proportional to the value of capacitance Cs. It follows that the value of the output current from transistor T1 will also be proportional to the value of capacitance Cs. The thin film transistor T1 is, therefore, being controlled in dependence upon the value of the capacitance arising at the sample electrode 10 resulting from the receipt by the sample electrode of the sample to be identified, i.e. a portion of the fingerprint on the fingertip.

The current on output line 34 is fed to the multiplex and amplification circuit 20. In the multiplex and amplification circuit 20, a transistor T1 is provided with a select signal from the second column select register 22 simultaneously with the column select signal on line 32. A bias voltage V_{bias} is provided to the gate electrode of transistor T5. In this manner the output current on line 34 can be amplified and multiplexed onto output 24 by appropriate selection of transistor T1. Likewise, the output current from other sensor cells can also be multiplexed onto output 24.

It will be appreciated that in the case when the sensor 2 comprises fingerprint recognition apparatus, a fingertip placed into contact with the sensor will have ridges of the fingerprint pattern in contact with certain sample electrodes and troughs of the fingerprint pattern in contact with other sample electrodes. Assuming that a fingerprint ridge is received by electrode 10 and a fingerprint trough is received by electrode

10a, the value of capacitance Cs for the sensor cell 4a will differ from the value of capacitance Cs for the sensor cell 4b. The same applies for other sensor cells in the array receiving ridge or trough portions of the fingerprint pattern. Typically, the sensor 4 may comprise a 200 x 300 sensor cell array. Hence, with appropriate timing of the signals from the row select register 14, and column select registers 16 and 22, the sensor cells of the array can be sequentially scanned and the multiplexed output signals of the sensor cells appearing on output 24 can be fed to a store. A comparator may compare the stored values for the samples with reference values and, as a result of such comparison, the fingerprint may be identified. The output signals on output 24 may also be fed to a display for displaying an image of the fingerprint as sensed by the sensor 2.

Preferably the multiplex and amplification circuit 20 is fabricated integrally with the sensor 2, in which case the transistors of the circuit, of which transistors T1 to T5 are shown, may also comprise TFT's on a common substrate 36 with the sensor 2. The transistor T6 for each sensor cell may also comprise a TFT. The substrate 36 may comprise any suitable support material but, advantageously, if all of the transistors of the sensor 2 are fabricated as TFT's, the substrate 36 may preferably comprise plastics material.

Although the steady state detection sensor shown in Figure 1 has been described with reference to a fingerprint recognition apparatus, it may also be used as a biosensor to detect or recognise biomaterials in solution, such as DNA or antibodies. In this case, a number of electrodes are provided which receive the substance in solution. The values of capacitance arising from the substance can be compared with known reference values in order to identify the particular substance.

Figure 2 shows an alternative embodiment for a sensor cell in accordan

ce with the present invention. The sensor cell shown in Figure 2 operates in a 'transient detection' mode in which a time constant determined by, for example, the value of capacitance arising from an electrode receiving a DNA sample for identification, is used to identify the sample.

In the sensor cell 4 shown in Figure 2, a switching transistor T7 is coupled to the electrode 10 and a node P provided between the transistor T7 and electrode 10 is coupled to the gate electrode of the thin film transistor T1. Select line 40, write line 42, and read line 44 are provided for respectively providing select signal V_{select}, preset signal V_{preset} and read signal V_{read}. A multiplex and amplifier circuit 20 is provided for providing an output signal on output 24.

Operation of the circuit shown in Figure 2 will be described with reference to identification of a DNA sample in solution. However, it should be understood that the transient detection circuit shown in Figure 2 can also be used for fingerprint recognition, in a similar manner to that described with reference to Figure 1. In the case of fingerprint detection, reference electrode 46 of Figure 2 would be constituted by the surface of the fingertip and the voltage V_{ref} of Figure 2 would be provided by the charge occurring on the surface of the fingertip.

At the start of an operating cycle the transistors T1 and T7, which may both comprise TFT's, are in a non-conducting or OFF condition. The electrode 10 is arranged as an electrode in a suitable reservoir into which is placed the DNA in solution. The DNA can be immobilised and is therefore received by the electrode 10 and, as a result, a capacitance value C_A arises between the sample electrode 10 and the reference electrode 46.

A preset cycle is initiated in which the switching transistor T7 is switched from a non-conducting condition to a conducting condition by the application of the voltage V_{select} to the gate electrode of transistor T

7. Simultaneously, the preset voltage V_{preset} is afforded to the source electrode of transistor T7 and the read voltage V_{read} is afforded to the source electrode of transistor T1. When transistor T7 is switched ON, the voltage at node P rises to the level of preset voltage V_{preset} and when the voltage at node P exceeds the threshold voltage of transistor T1, the transistor T1 will switch ON with the current at the output of transistor T1 being a function of the voltage at node P (the gate electrode of transistor T1).

A read cycle is then initiated by terminating the select voltage V_{select}, causing transistor T7 to switch back to a non-conducting or OFF condition. When transistor T7 is switched OFF, the voltage on node P reduces by leaking away through transistor T7 and the rate or the time constant for this leakage to occur depends on the value of capacitance C_A, which is dependent upon the identity of the DNA sample received by the sample electrode 10. As the voltage at the node P reduces in magnitude, there is a related decrease in the current at the output of thin film transistor T1, which is fed to the multiplex and amplification circuit 20. When the voltage at node P reduces to below the threshold voltage of transistor T1, transistor T1 switches OFF to further reduce the current fed to the multiplex and amplifier circuit 20 to that of a leakage current flowing through transistor T1. It will be realised from the above description that transistor T7 is used as a digital switching transistor whereas the transistor T1 acts as an analogue voltage to current converter. Therefore, by monitoring the current at the output of transistor T1, which is dependent on the value of capacitance C_A, the identity of the sample received by the electrode 10 can be determined.

For use as a biosensor, pairs of such sensor cells, as shown in Figure 2, may be provided, one cell of a pair acting as the sample cell and the second of the pair acting as a reference cell in which no reaction has

occurred.

When the sensor cells shown in Figures 1 and 2 are for use as chemical or biosensors, for example a DNA sensor, the chemical or biomaterials to be identified most first be written into the cells and onto the reference electrodes. This can be regarded as a write phase for the cells and preferably occurs when the devices are fabricated. Inkjet heads may conveniently be used to deposit the chemical or biomaterials and deposition onto the electrodes may be assisted by electrodeposition in which a charge is applied to the electrode so as to attract the material being deposited to its desired deposition site.

Figure 3 shows an embodiment of a semiconductor structure which may be used to provide the thin film transistor T1, the electrode 10, and the reference capacitor Cr.

The TFT structure of Figure 3 comprises a layer of polysilicon 48 supported by the substrate 36, which preferably is of plastics or soda glass material. The gate electrode 26 is formed over the polysilicon layer 48, separated from the polysilicon layer by an insulating layer 50 of silicon dioxide. Passivation layers 52, 54 overlie the gate electrode 26.

The insulating layer 50 and the gate electrode 26 are arranged to extend beyond the region of the polysilicon layer 48 to overlie a buried region 56 of metal or doped polysilicon formed on the substrate 36. The passivation layers 52, 54 are provided with a well extending down to expose the gate electrode 26 in an area overlying the buried region 56. The electrode 10, which may comprise gold, silver or platinum, is formed in the well extending down into contact with the gate electrode 26. In this manner, the reference capacitor is provided between the buried region 56 and the gate electrode 26. For illustrative purposes, the reference capacitor is shown in phantom in Figure 3.

Also, because the structure shown in Figure 3 incorporates a TFT and n

ot a silicon substrate transistor, the electrode 10 can be positioned so that it is offset from the TFT without conflicting with the need to achieve maximum packing density on the expensive silicon substrate material. The electrode 10 is therefore arranged so that it does not overlie the gate regions of the TFT. As such, the electrode 10 can be of enlarged size to improve device sensitivity but also the encapsulation required to isolate the TFT from the wet environment occurring at the electrode can be fabricated more easily and more reliably because there is no requirement to achieve a high packing density of devices on an expensive substrate.

It can be seen from Figure 3 that the structure provides a compact arrangement incorporating the thin film transistor T1, the electrode 10, and the reference capacitor Cr. Hence, the structure can be incorporated into the steady state detection sensor cell shown in Figure 1. When the sample to be identified is received by the electrode 10, the value of capacitance C_S arising between the electrode 10 and the sample, shown diagrammatically in Figure 3, forms in combination with the integral reference capacitor Cr, the capacitance divider circuit described with reference to Figure 1, which controls the operation of the TFT.

For the transient detection sensor cell shown in Figure 2, where the reference capacitor is not required, the buried region 56 can be omitted.

As stated above, a concern with polysilicon TFT's is threshold voltage variation. Figure 4 illustrates an alternative circuit for a sensor cell which compensates for this variation and provides a comparable output from the TFT's across a large area substrate.

In the sensor cell of Figure 4, the thin film transistor T1 is coupled via a switch S to either a constant current supply I_{Source} or an output

line. An additional transistor T8, which operates as a switching transistor, is connected between the gate and drain electrodes of thin film transistor T1, and the reference capacitor Cr is connected between the gate and source electrodes of transistor T1. The electrode for receiving the sample to be identified (not shown in Figure 4) is also coupled to the gate electrode of transistor T1. The sample capacitance Cs forms, therefore, a capacitance divider with the reference capacitor Cr, in a similar manner to that described with reference to Figure 1.

When transistor T8 is turned ON, the gate to source voltage V_{GS} and drain to source voltage V_{DS} for transistor T1 will be equal. Under such conditions, the operational characteristic for transistor T1 is simplified, as shown in Figure 5. With switch S in position "1", the current from the constant current source I_{Source} is pulled through transistor T1, which results in a voltage drop V_{DSref} across transistor T1. Because transistor T8 is ON, (and hence V_{GS} is equal to V_{DS} for transistor T1), the voltage drop V_{DSref} appearing across transistor T1 is stored in the reference capacitor Cr.

Threshold variation in thin film transistor T1 may result in a shift in the simplified operational characteristic curve (when V_{GS} is equal to V_{DS}) for transistor T1, as shown in Figure 6. The value of the current flowing through transistor T1 is constant as it is being supplied from the constant current source, I_{Source}. Any threshold variation will therefore result in a change in the voltage drop V_{DSref} occurring between the source and drain electrodes of transistor T1. The voltage V_{DSref} is stored in the reference capacitor Cr and, therefore, the voltage V_{GS} between the gate and source electrodes of transistorT1 is precharged to this value. In this way, transistor T1 is preset to a known point on its characteristic.

If the switch S is now moved to position "2" and T8 is switched OFF, i

nitially the current I_{out} on the output line will be equal to the current from the constant current supply I_{Source}, as it is governed by the voltage at node P, which in turn is governed by the voltage stored on the reference capacitor Cr. If voltage source V_{ref} is now pulsed, the voltage at node P increases and pulses in sympathy with the voltage V_{ref}. The current I_{out} at the output line will also pulse in sympathy with the increase in the voltage at the node P.

The reference capacitor Cr and the capacitance Cs form a capacitive divider and, hence, the increase in the voltage at node P when the voltage source V_{ref} is pulsed will be determined by the relative capacitance values of Cr and Cs. The increase in the output current I_{out} from its initial value equal to the current from the constant current supply I_{Source} can be measured to quantify the value of capacitance Cs, which is indicative of the sample received by the sample electrode.

It will be appreciated that the switch S may be provided by solid state switching means, such as thin film transistors on the substrate 36.

Figure 7 illustrates a further embodiment of the present invention where the sensor can be used as a pH sensor. The structure shown in Figure 7 is very similar to the structure shown in Figure 3, so wherever possible like reference numerals have been used to indicate like parts of the structure.

In the structure shown in Figure 7, a well 58 is provided in the passivation layer 52 to expose the gate electrode 26. The passivation layer 54 is provided extending as a continuous layer over the passivation layer 52 and the gate electrode 26 in the well 58 to provide a relatively thin layer of passivation material 60 overlying the gate electrode. When a sample to be identified in the form of a solution, such as urea or glucose for example, is placed into the well 58 and into contact with the layer 60, ions in the solution are located near to the layer 60 and prote

ns, indicated with + symbols in Figure 7, are absorbed on surface 62 of layer 60. Because the layer 60 is very thin this charge transfers to the gate electrode 60 and provides therefore a voltage which controls the operation of the TFT transistor constituted by gate electrode 26, polysilicon region 48 and silicon dioxide layer 50. The charge created in the layer 60 by adsorption of the ions onto the surface 62 is related to the pH of the solution deposited into the well 58. Hence, by monitoring the output from the TFT the substance in solution can be identified.

The aforegoing description has been given by way of example only and it will be appreciated by a person skilled in the art that modifications can be made without departing from the scope of the present invention.

For example, the sensor cells have been described with reference to detection of chemical or biomaterials in liquid form. However, it should also be realised that the sensor cells may be used to analyse fluids other than liquids, such as gases.

Furthermore, the present invention has been described with reference to one sensor cell being used to analyse a particular chemical or biomaterial sample. However, as the TFT's can be reliably fabricated into very large area arrays in comparison to silicon substrate devices, the matrix of sensor cells making up the sensor may be provided with several sensor cells, each having a particular DNA string written onto the reference electrode. If such cells are arranged in spaced relationship across the array, the output signals from these sensor cells having a common reference material, such as a DNA string, written onto the reference electrode may be averaged by appropriate circuitry so as to provide enhanced accuracy of analysis. The analysis circuitry may also be fabricated on the substrate using TFT's. Therefore, in essence, the sensor may be provided with a number of 'duplicate' sensor cells, each arranged to identify the common DNA string. This is made possible through the use of TFT's

because a very large number of sensor cells can be incorporated into a very large area array.

4.Brief Description of Drawings

Figure 1 illustrates a sensor according to a first embodiment of the present invention;

Figure 2 illustrates a sensor according to a second embodiment of the present invention;

Figure 3 illustrates a structure for a sensor cell for use in the sensor shown in Figure 1;

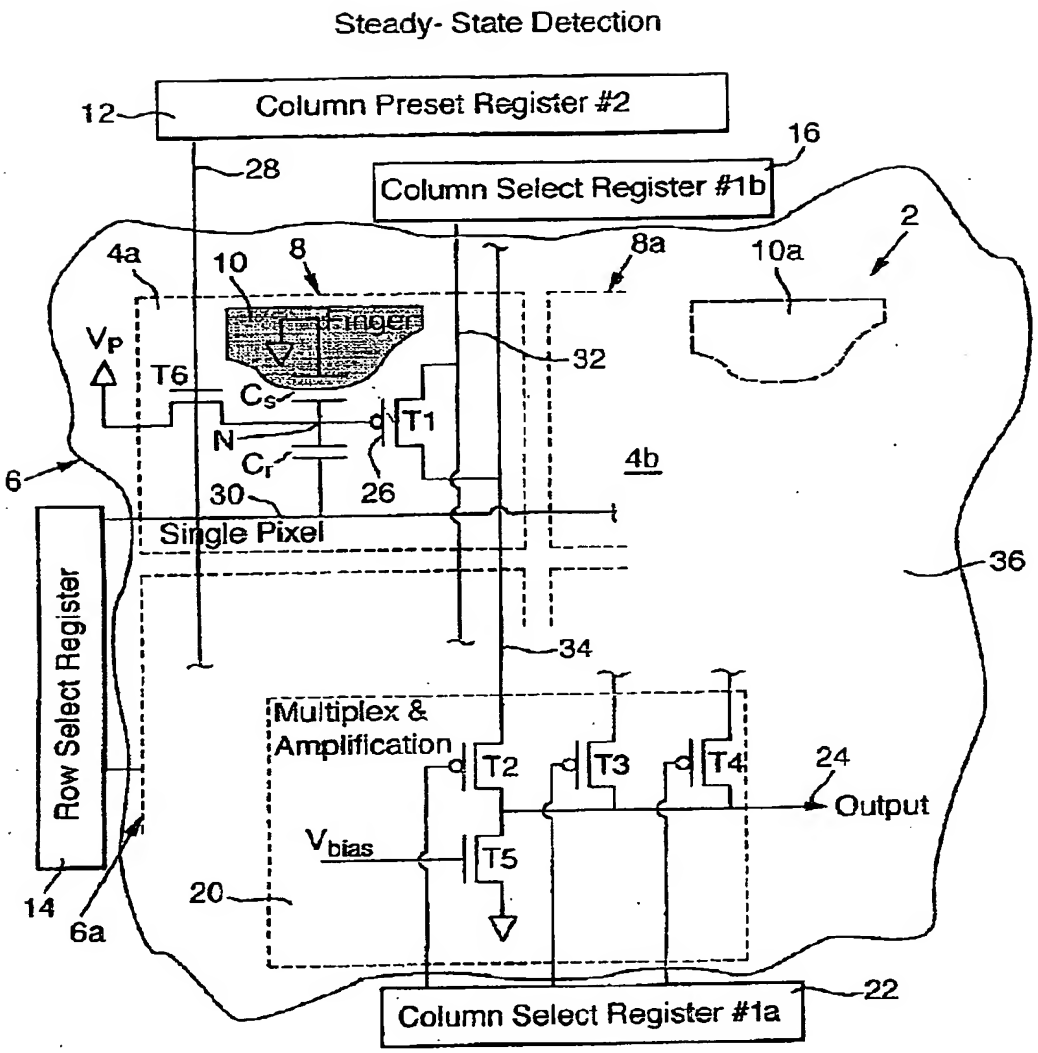
Figure 4 illustrates a sensor cell including threshold voltage variation for use in the sensor shown in Figure 1;

Figure 5 illustrates a simplified operational characteristic for the thin film transistor of the sensor cell shown in Figure 4;

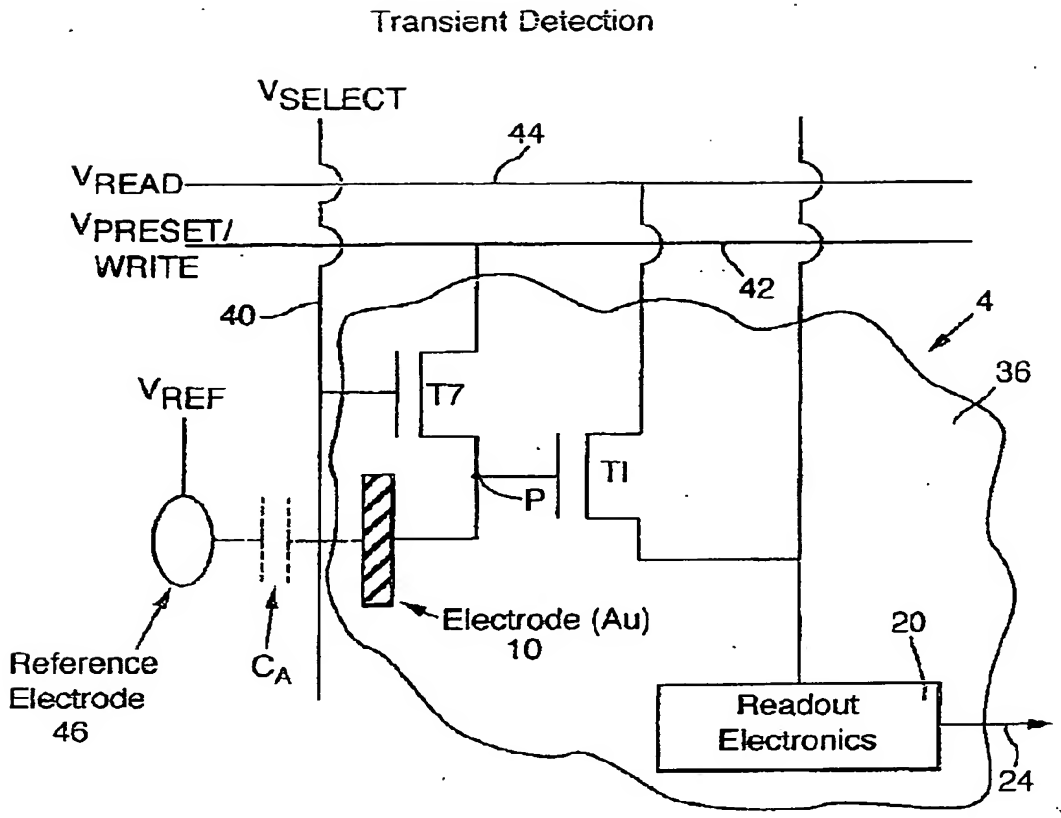
Figure 6 illustrates the variation of the simplified operational characteristic shown in Figure 5, with variation of the threshold voltage of the thin film transistor; and

Figure 7 illustrates an alternative structure for a sensor cell for use as a pH sensor in accordance with the present invention.

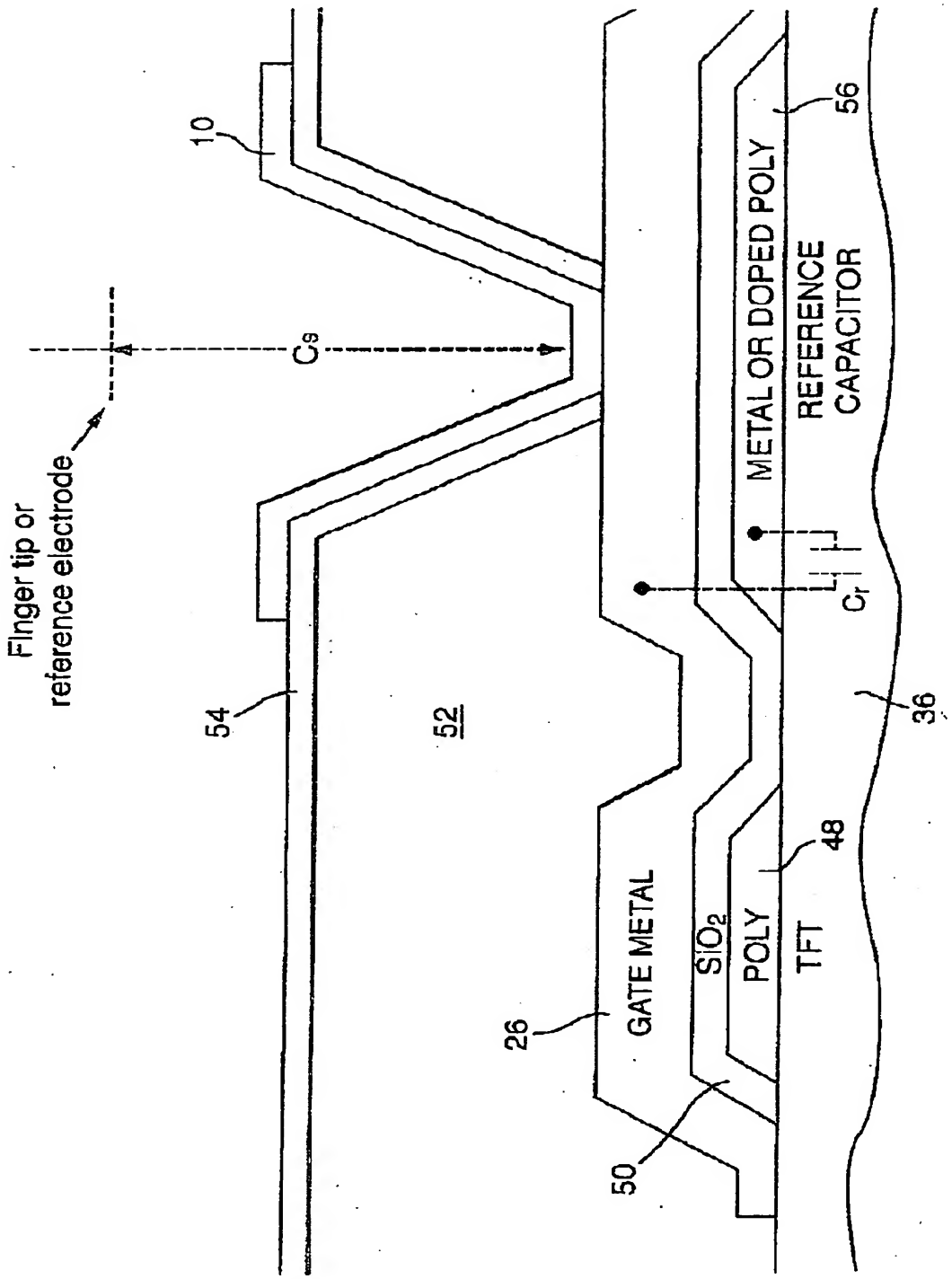
[Fig. 1]


Steady- State Detection
12
Column Preset Register #2
28
16
Column Select Register #1b
2
4a
10
8
8a
10a
Charge
V_P
T6
C_S
32
N
T1
C_T
26
4b
6
30
Single Pixel
36
Row Select Register
34
Multiplex &
Amplification
T2
T3
T4
24
Output
V_{bias}
T5
20
14
6a
22
Column Select Register #1a

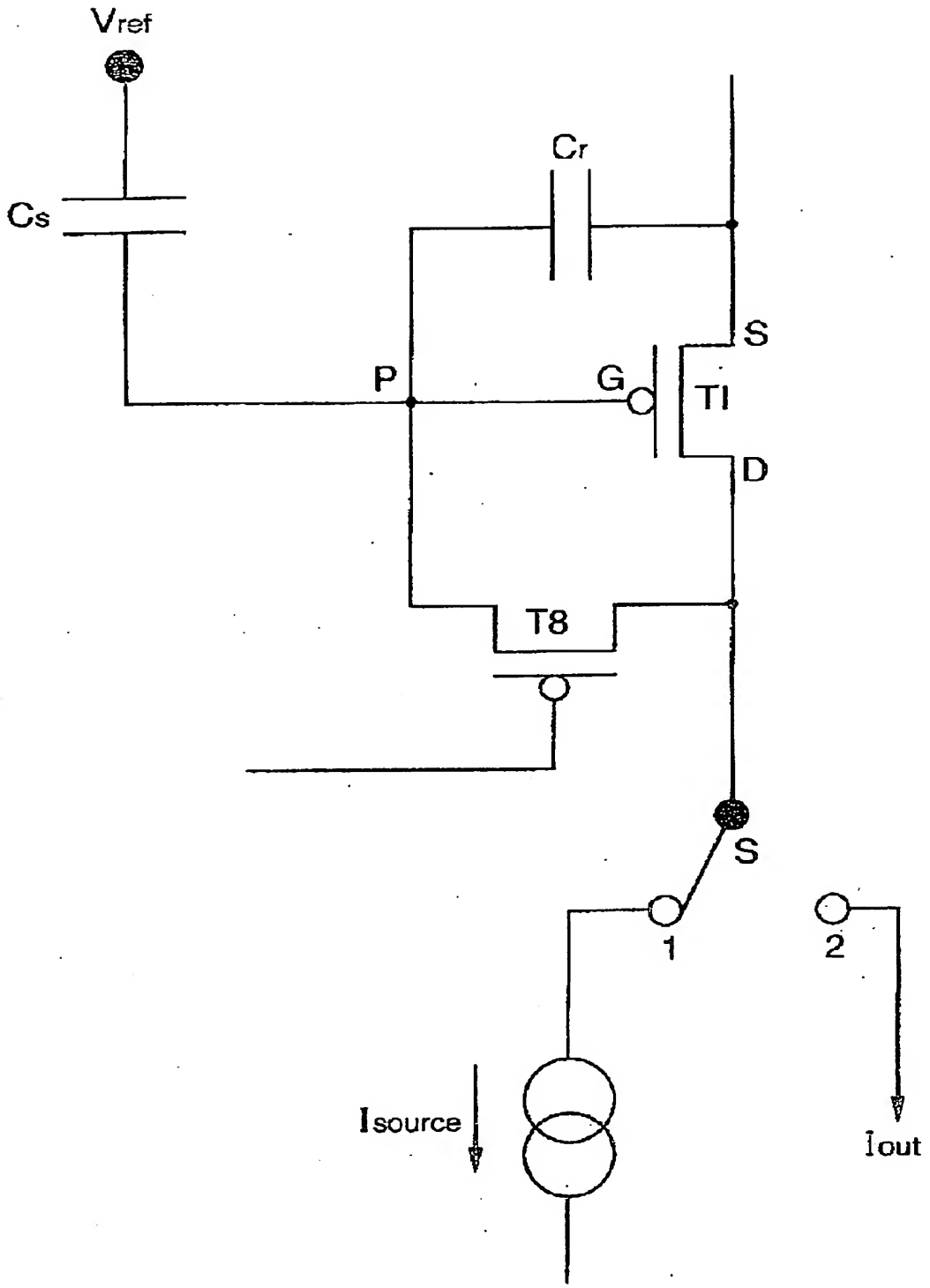
【Fig. 2】


Transient Detection
VSELECT
44
VREAD
VPRESET/
WRITE
42
40
4
36
VREF
T7
T1
P
Electrode (Au)
10
20
Reference
Electrode
46
CA
Readout
Electronics
24

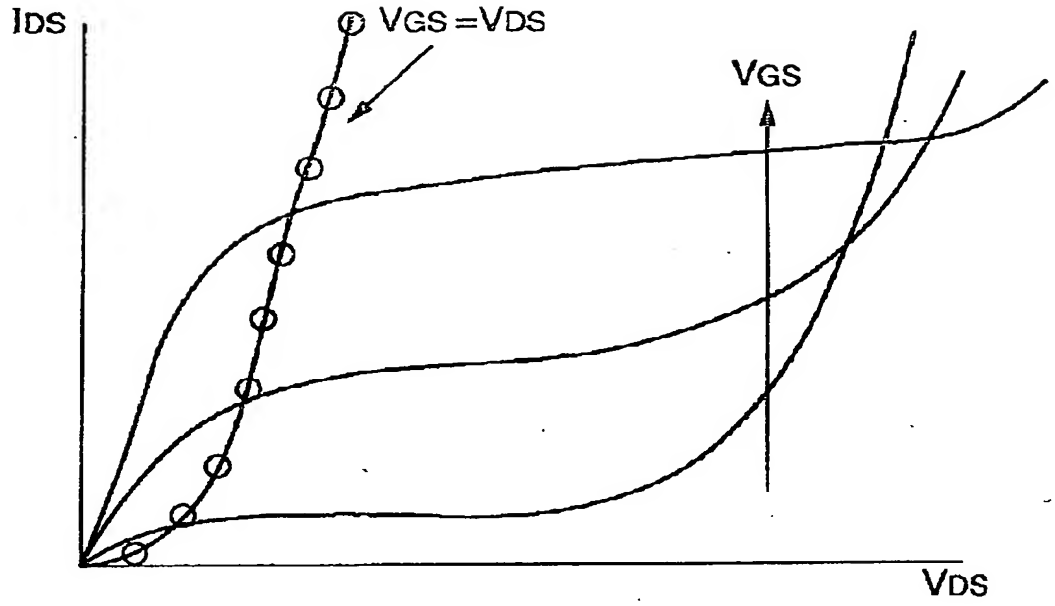
[Fig. 3]


10
C_s
Finger tip or reference electrode
54
52
56
METAL OR DOPED POLY
REFERENCE CAPACITOR
C_r
36
48
TFT
POLY
SiO_2
GATE METAL
26
50

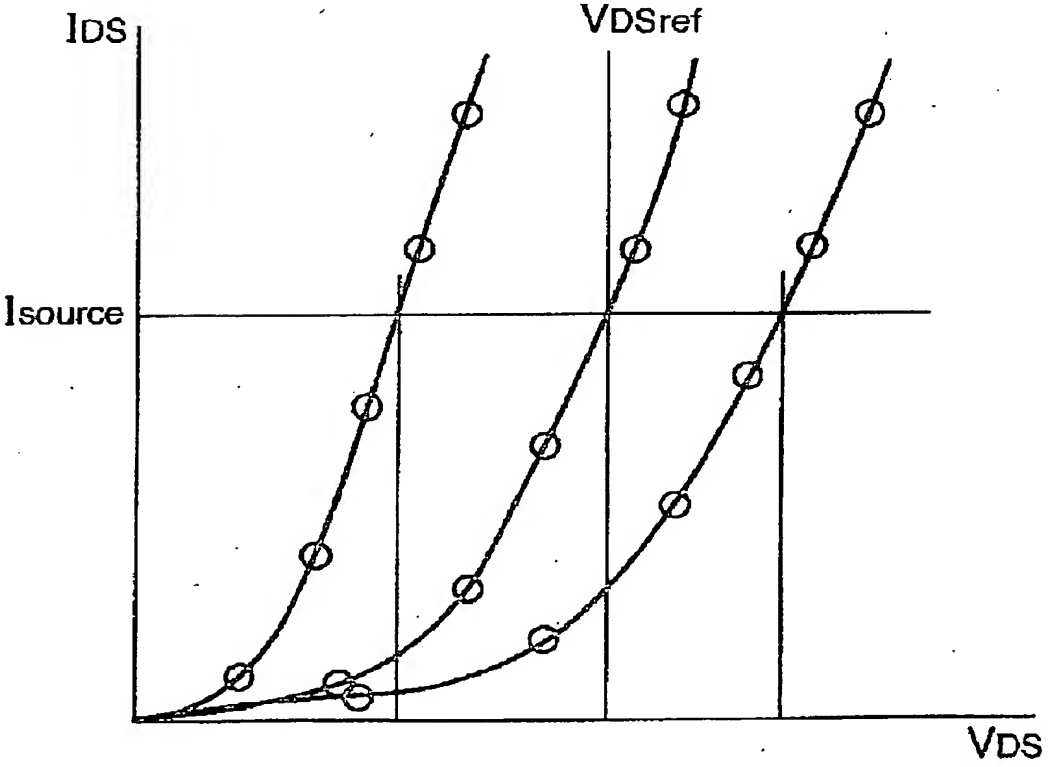
[Fig. 4]



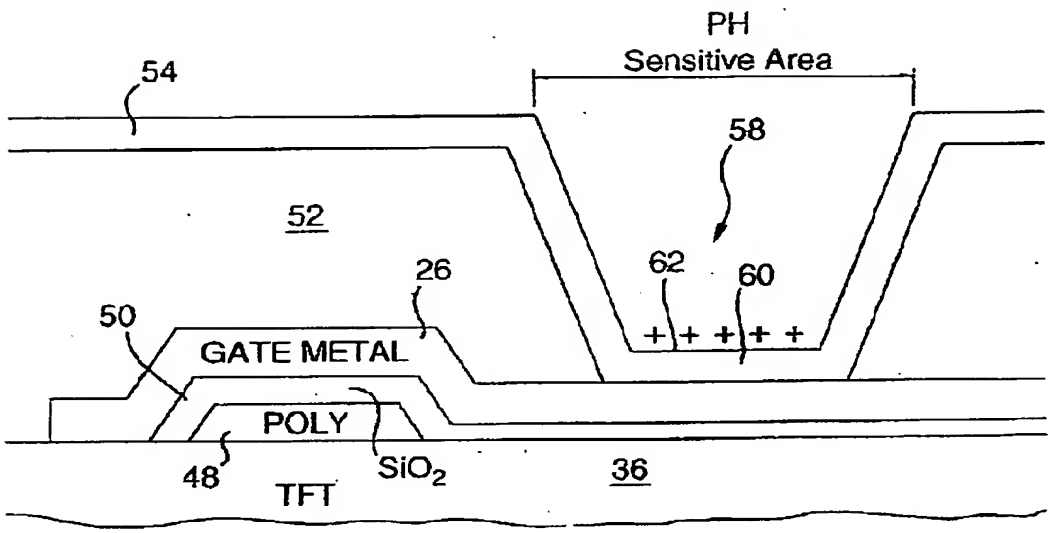
【Fig. 5】



【Fig. 6】



【Fig. 7】



1. Abstract

A sensor cell comprises receiving means, which may be in the form of a n electrode 10 coupled to the gate electrode of a thin film transistor T 1. In one form of the invention a voltage supplied to the gate electrod e of the transistor T1 via a switching transistor T7 is controlled in de pendence upon the value of capacitance C_A arising at the electrode from receipt of a sample for identification. Thus, the operation of transist or T1 can be used to identify the sample received by the electrode 10.

2. Representative Drawings

Fig. 2